

# ***LCFC Confidential***

## ***CE475 NM-A861 Rev1.0 Schematic***

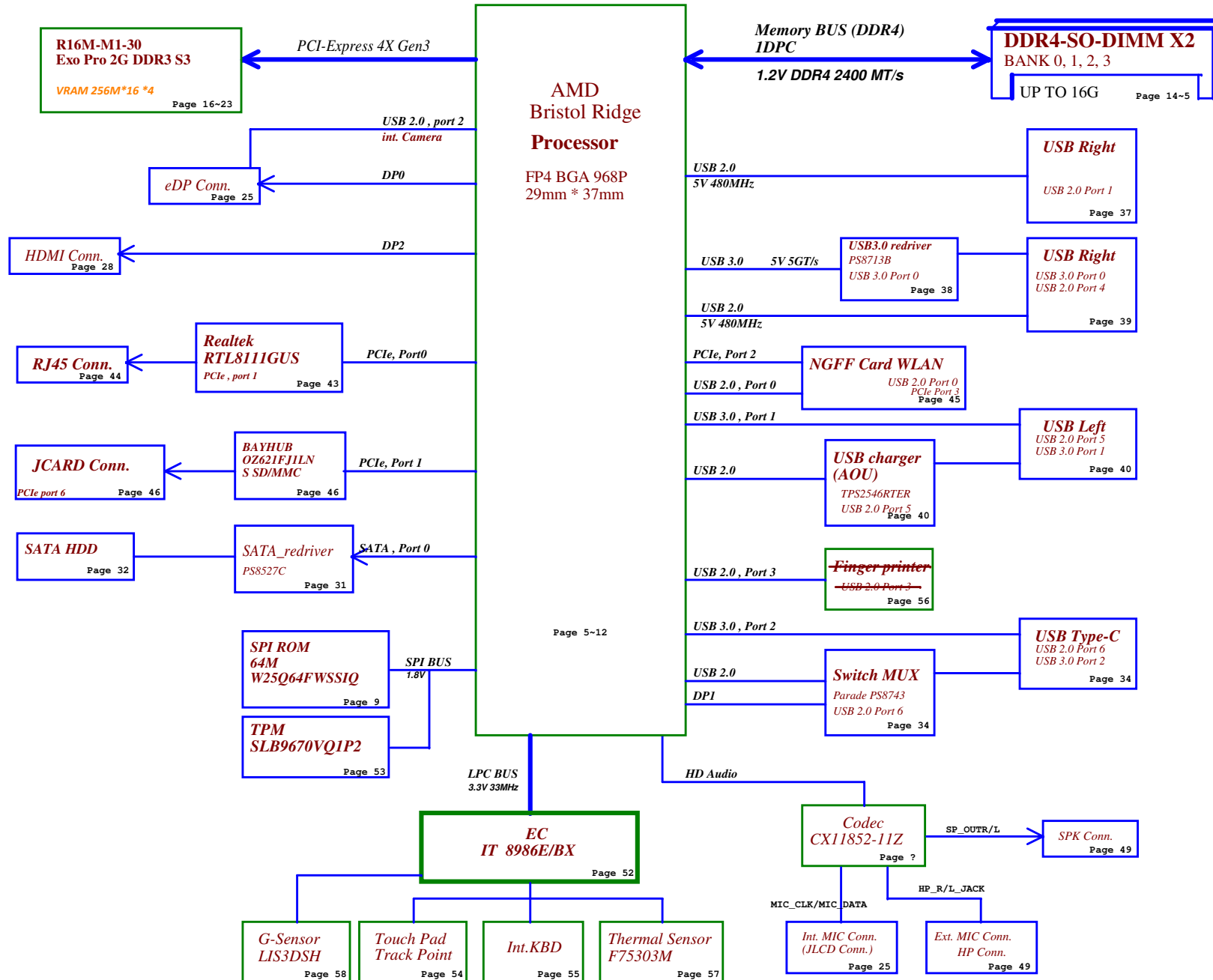
***AMD Bristol Ridge Processor with DDR4***

***R16M-M1-30 with DDR3 4GB***

***2016-7-20 Rev1.0***

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/10/5	Deciphered Date	2016/12/31	COVER PAGE	
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# AMD Bristol Ridge FP4



# Voltage Rails ( O --> Means ON , X --> Means OFF )

Power Plane / State	B+	+3VALW +5VALW	+1.2V	+5VS +3VS +1.5VS +1.05VS +0.6VS +VCC_CORE +VGA_CORE +3.3VS_VGA +1.8VS_VGA +1.35VS_VGA +1.05VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

ZZZ1 PCB@  
NM-A861  
DA80002700

STATE	SIGNAL	SLP_A#	SLP_S3#	SLP_S4#	SLP_S5#	EC_ON	SUSP#
S0		HIGH	HIGH	HIGH	HIGH	ON	ON
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF

## USB2 Port

Port	Device
1	NGFF Card
2	USB port3
3	Int. Camera
4	Finger Printer
5	USB port1
6	USB (AOU)
7	USB Type-C
8	X

## USB3 Port

Port	Device
1	USB port1
2	USB (AOU)
3	USB Type-C
4	X

## PCIE Port

Port	Device
1	LAN
2	CardReader
3	WLAN
4	X
5	GPU
6	GPU
7	GPU
8	GPU
9	X
10	X
11	X
12	X

## SATA Port

Port	Device
1	HDD
2	X

## SMBUS Control Table

	SOURCE	Main VGA	BATT	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	CP Module	Security ROM	CCG2	G-Sensor
EC_SMB_CK1 EC_SMB_DA1	IT8986F +3VL	X	V +3VALW	X	X	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8986F +3VS	X	X	X	X	X	X	X	X	V +3VALW	X
EC_SMB_CK3 EC_SMB_DA3	IT8986F +3VS	V +3VS_VGA	X	X	X	V +3VS	V +3VALW_PCH	X	X	X	V +3VALW

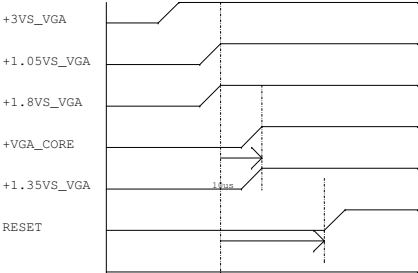
VGA and DDR3 Voltage Rails (JET TOPAZ GPIO)

20151022

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	N/A	
GPIO5	IN	-	GPIO5_AC_BATT
GPIO6	IN	-	GPIO6
GPIO7	OUT	N/A	
GPIO8	OUT	-	GPIO8_ROMSO
GPIO9	OUT	-	GPIO9_ROMSI
GPIO10	OUT	-	GPIO10_ROMSCK
GPIO11	OUT	N/A	
GPIO12	OUT	N/A	
GPIO13	OUT	N/A	
GPIO15	IN	N/A	SVI2_SVD
GPIO16	OUT	N/A	
GPIO17	OUT	N/A	
GPIO19	OUT	N/A	GPIO19_CTF
GPIO20	IN	IN	GPIO20
GPIO21	OUT	N/A	
GPIO22	OUT	N/A	GPIO22_ROMCSB
GPIO29	OUT	N/A	
GPIO30	OUT	N/A	

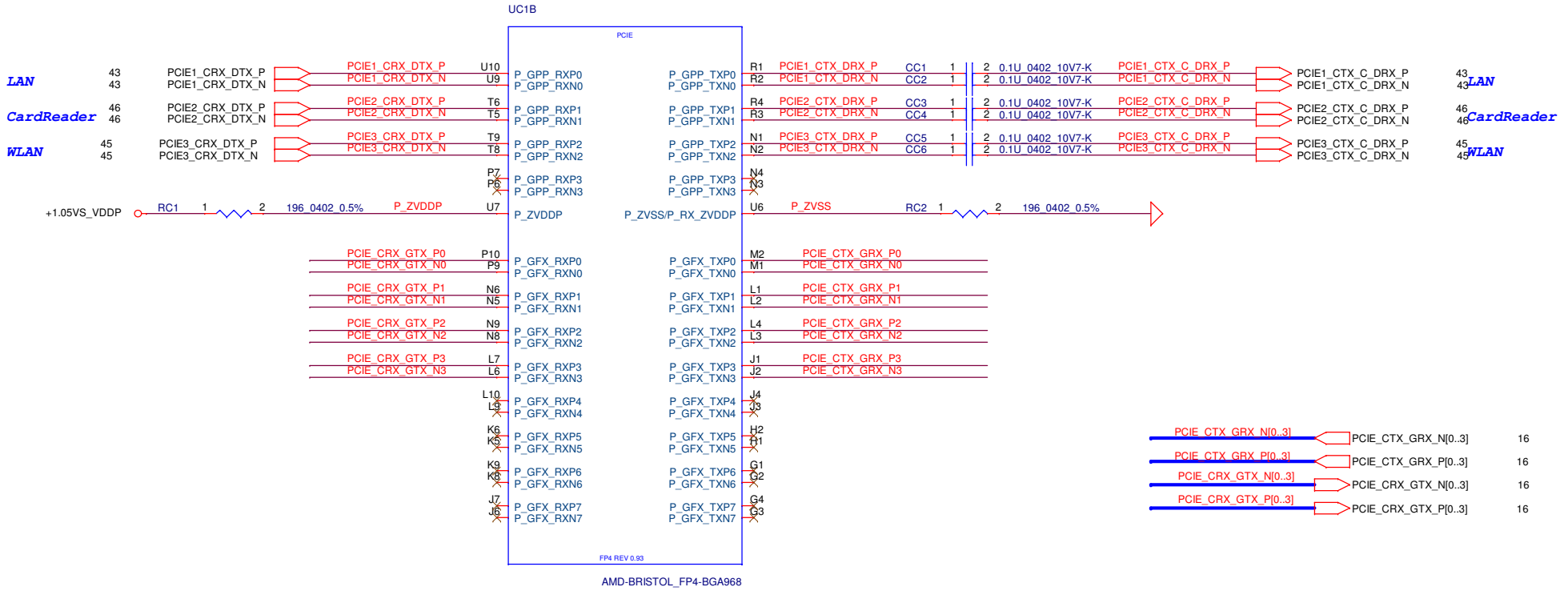
BOM Structure Table

BOM Structure	NOTE
EXO@	For GPU_EXO
MESO@	For GPU_MESO
DIS@	For GPU function
X76@	GPU VRAM Setting
TPM@	Trusted Platform Module(TPM)
UMA@	UMA SKU ID
DPRE@	DP re-driver function
SA@	SATA redriver function
RESA@	Disable SATA re-driver
HD@	HDMI repeater function
ME@	ME Connector
RF@	For RF function
EMC@	For EMI function
NVPRO@	For Non-VPRO function
VPRO@	For VPRO function
U31@	For U3 port1 redriver function
U32@	For U3 port2 redriver function
U33@	For U3 port3 redriver function
NU3R@	Bypass U3 port3 redriver
TYPEC@	TYPEC FUNCTION

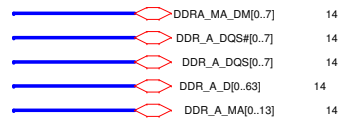
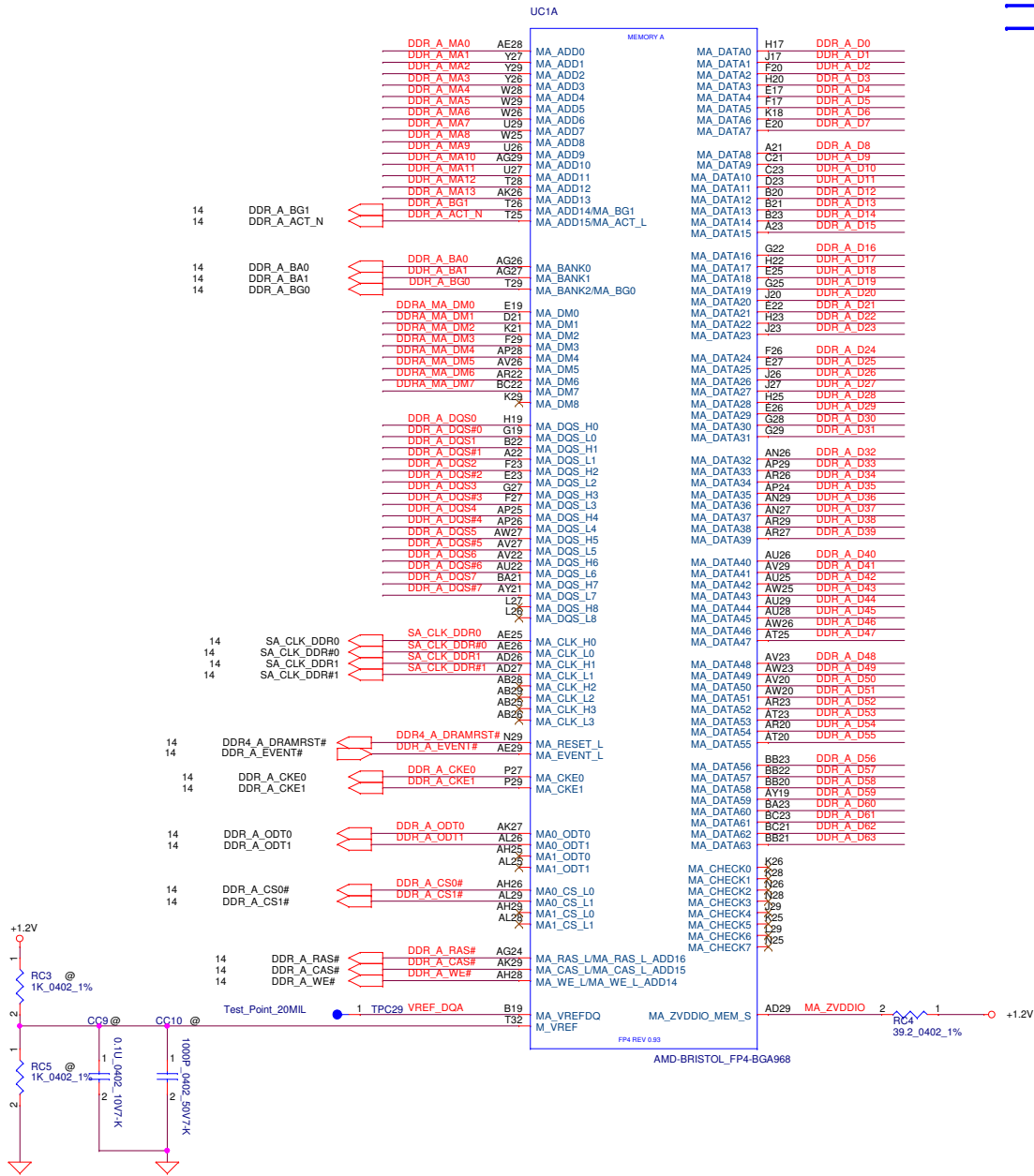


	Device ID
JET-XT	0x6664
TOPAZ XT	0x6900

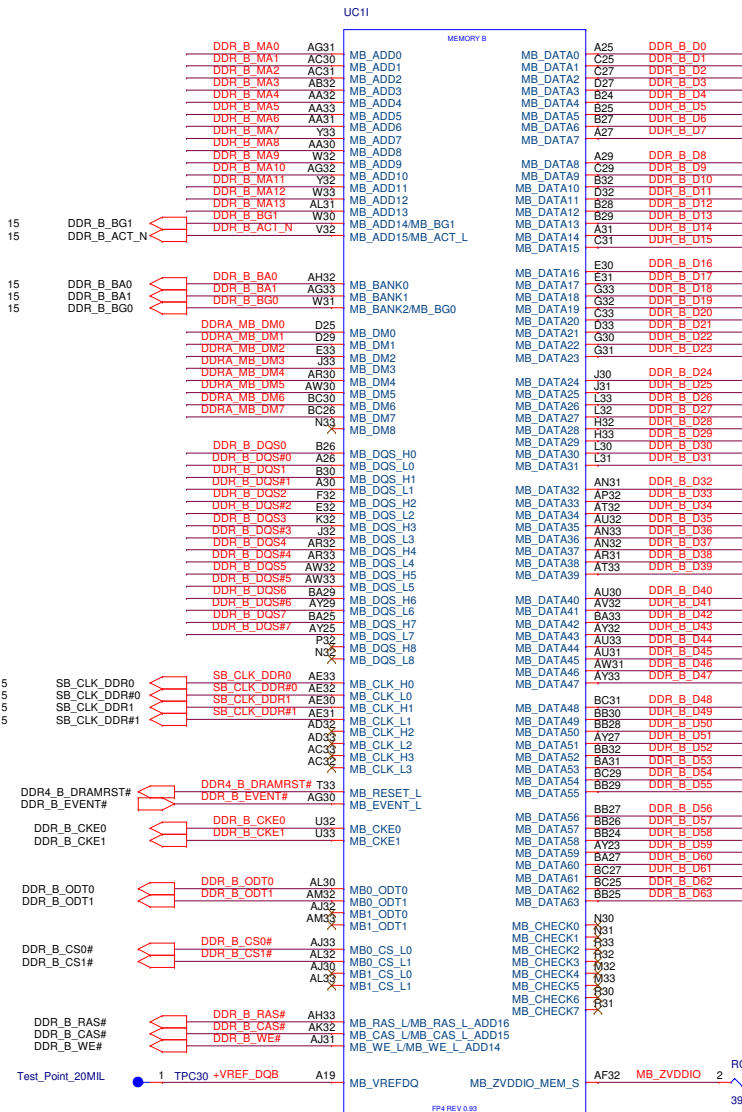
		RV104	RV105
Memory (GDDR3)			
Samsung	1G	SA22225SH30*4	PU 8.45K PD 2K
	2G	SA000063F00*4	PU 3.4K PD 10K
Hynix	1G	SA00005VS10*4	PU 4.53K PD 2K
	2G	SA00005YL10*4	PU 4.75K NC
Micron	1G	SA00005M100*4	NC PD 4.75K
	2G	SA000060I00*4	PU 3.24K PD 5.62K



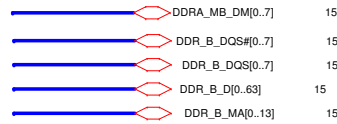
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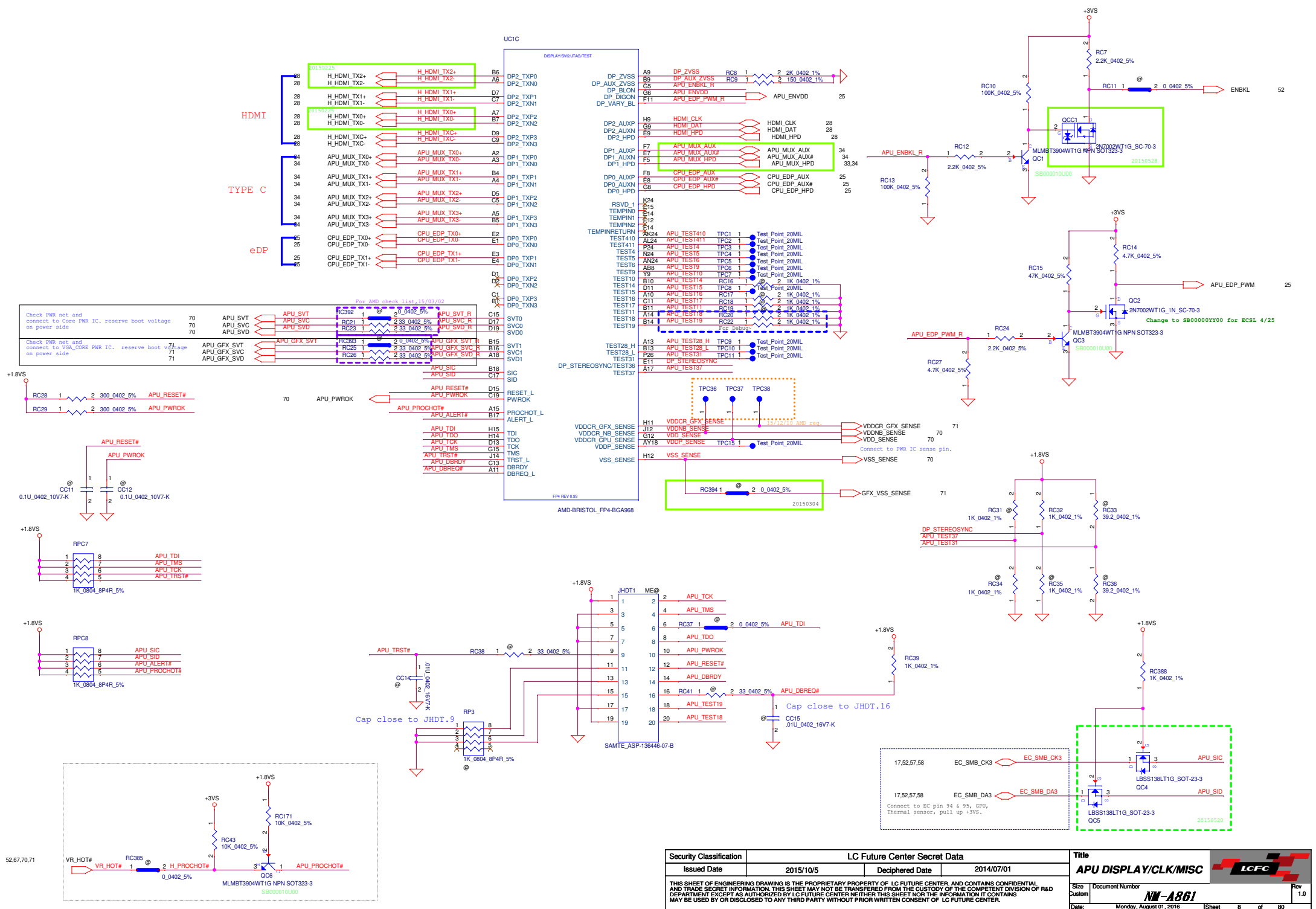
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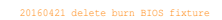
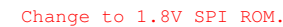


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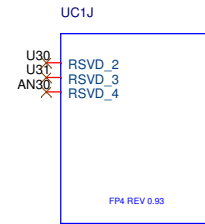
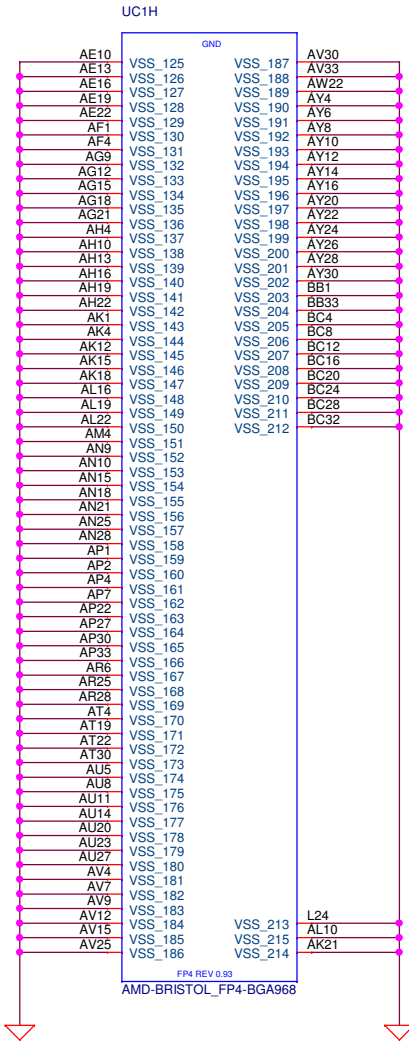
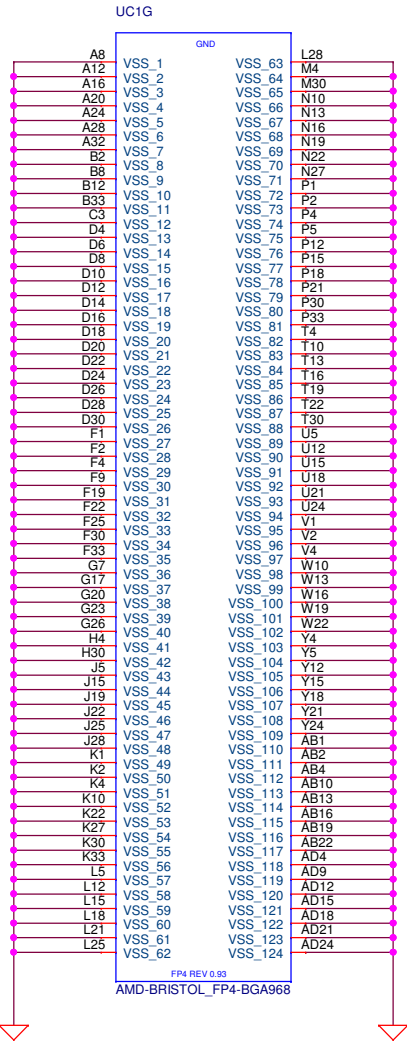



0 USB 3.0 System Port (AOU)



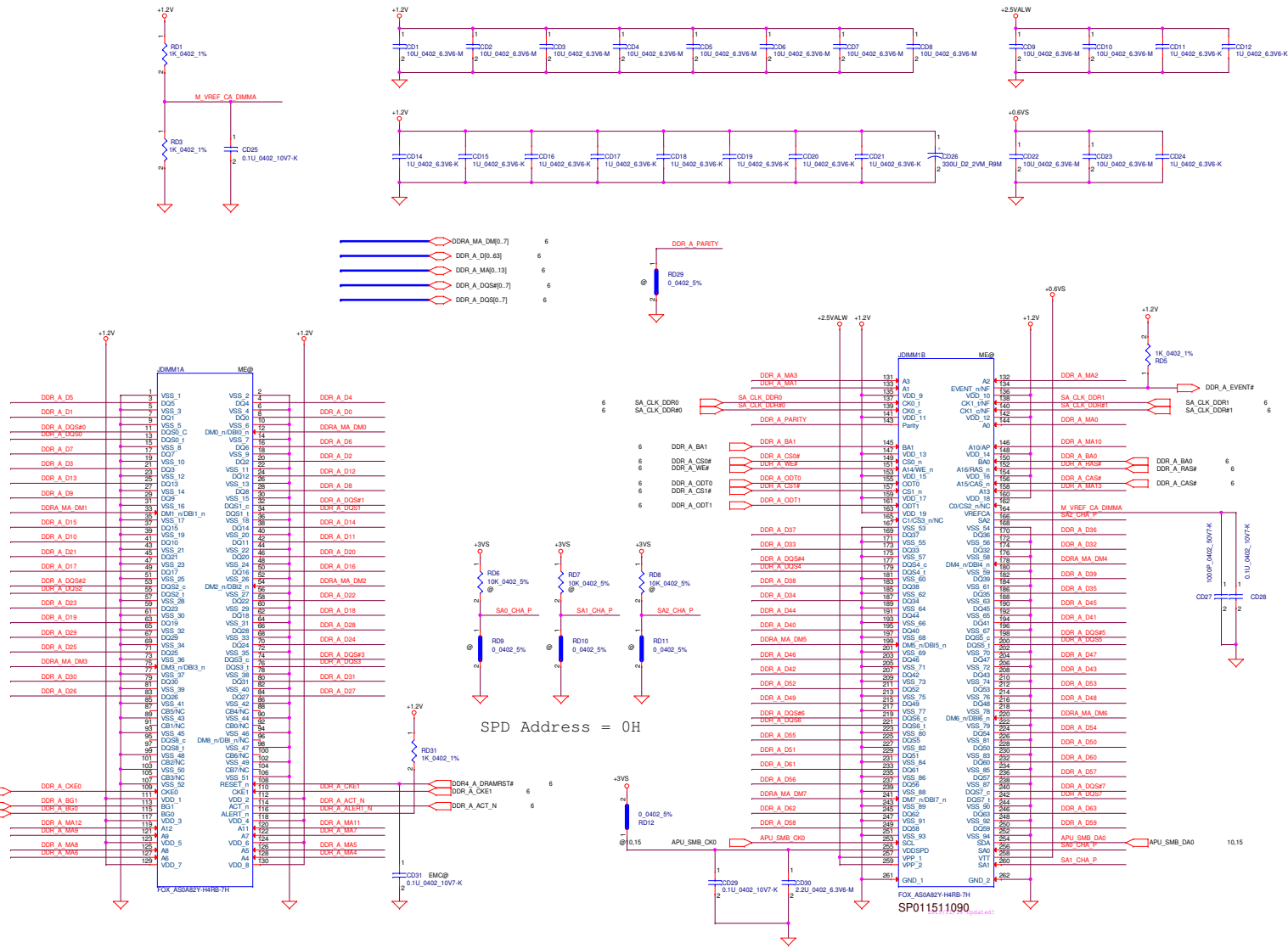


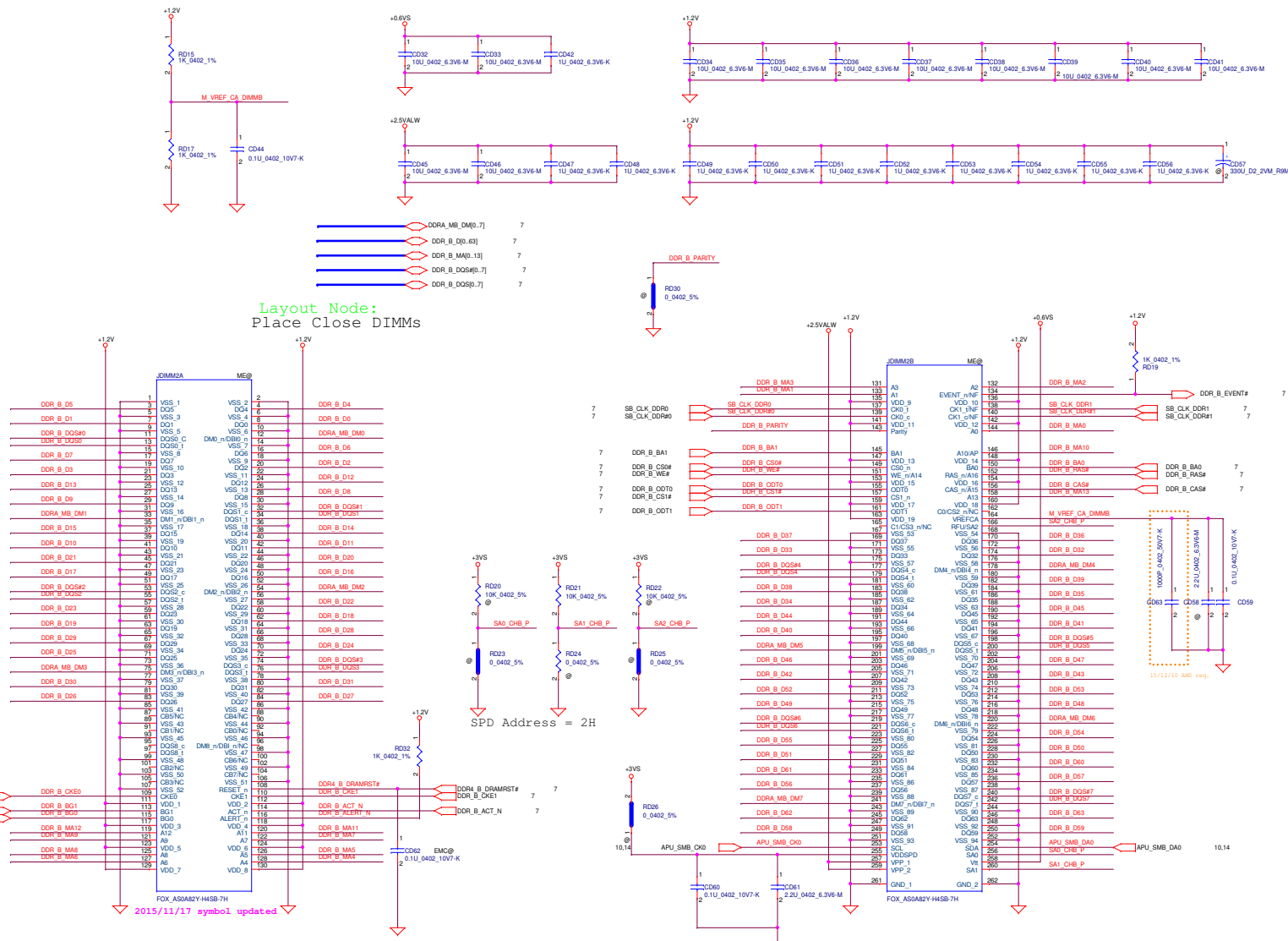




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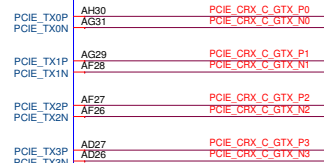
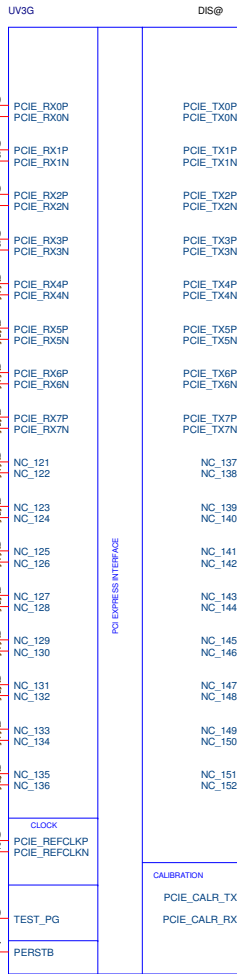
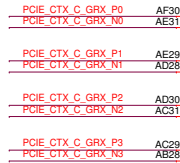
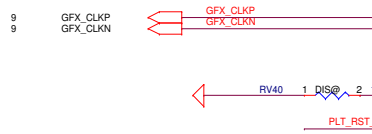
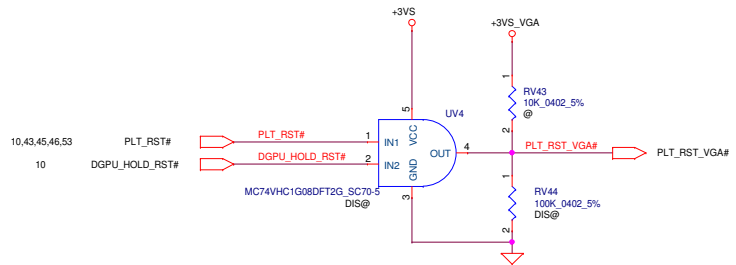
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D				D															
C				C															
B				B															
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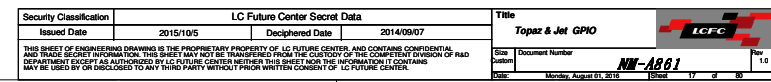


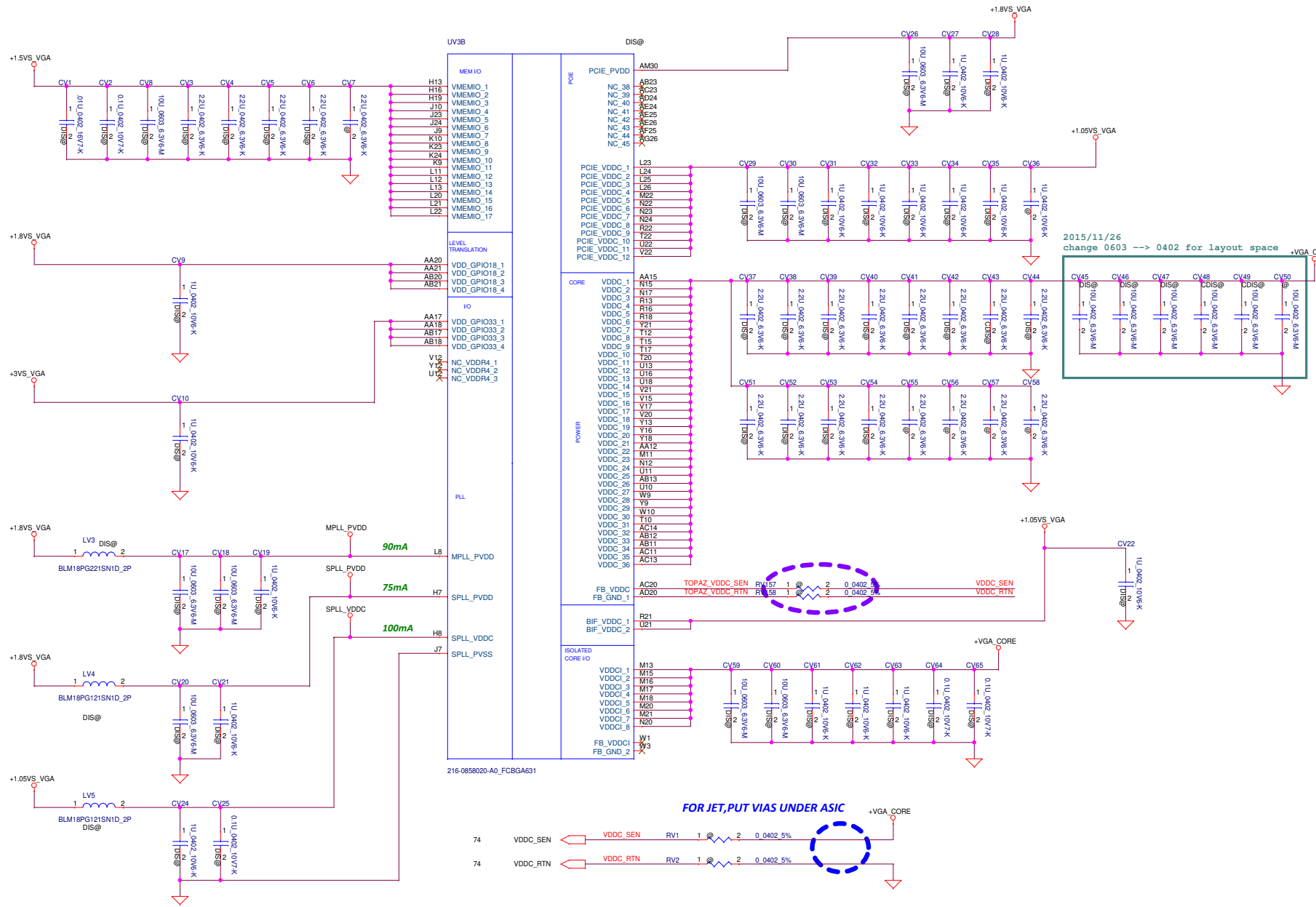
DIS@					
support GEN3:sonic20150211					
PCIE_CTX_GRX_P0	CV132	DIS@ 2	1	0.22U 0402 10V6-K	PCIE_CTX_C_GRX_P0
PCIE_CTX_GRX_N0	CV133	DIS@ 2	1	0.22U 0402 10V6-K	PCIE_CTX_C_GRX_N0
PCIE_CTX_GRX_P1	CV134	DIS@ 2	1	0.22U 0402 10V6-K	PCIE_CTX_C_GRX_P1
PCIE_CTX_GRX_N1	CV135	DIS@ 2	1	0.22U 0402 10V6-K	PCIE_CTX_C_GRX_N1
PCIE_CTX_GRX_P2	CV136	DIS@ 2	1	0.22U 0402 10V6-K	PCIE_CTX_C_GRX_P2
PCIE_CTX_GRX_N2	CV137	DIS@ 2	1	0.22U 0402 10V6-K	PCIE_CTX_C_GRX_N2
PCIE_CTX_GRX_P3	CV138	DIS@ 2	1	0.22U 0402 10V6-K	PCIE_CTX_C_GRX_P3
PCIE_CTX_GRX_N3	CV139	DIS@ 2	1	0.22U 0402 10V6-K	PCIE_CTX_C_GRX_N3



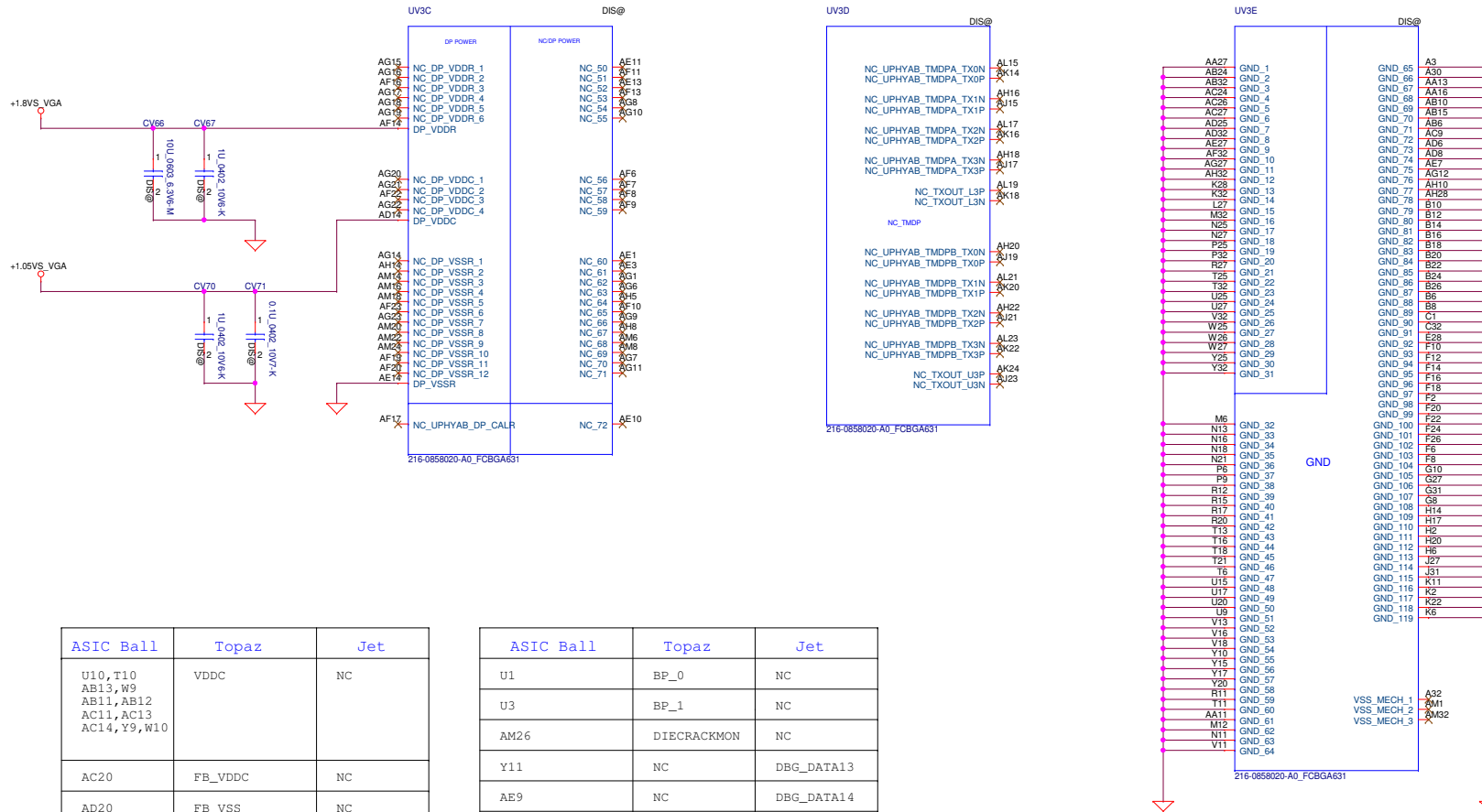
DIS@					
support GEN3:sonic20150211					
PCIE_CRX_GTX_P0	CV191	DIS@ 2	1	0.22U 0402 10V6-K	PCIE_CRX_C_GTX_P0
PCIE_CRX_GTX_N0	CV192	DIS@ 2	1	0.22U 0402 10V6-K	PCIE_CRX_C_GTX_N0
PCIE_CRX_GTX_P1	CV193	DIS@ 2	1	0.22U 0402 10V6-K	PCIE_CRX_C_GTX_P1
PCIE_CRX_GTX_N1	CV194	DIS@ 2	1	0.22U 0402 10V6-K	PCIE_CRX_C_GTX_N1
PCIE_CRX_GTX_P2	CV195	DIS@ 2	1	0.22U 0402 10V6-K	PCIE_CRX_C_GTX_P2
PCIE_CRX_GTX_N2	CV196	DIS@ 2	1	0.22U 0402 10V6-K	PCIE_CRX_C_GTX_N2
PCIE_CRX_GTX_P3	CV197	DIS@ 2	1	0.22U 0402 10V6-K	PCIE_CRX_C_GTX_P3
PCIE_CRX_GTX_N3	CV198	DIS@ 2	1	0.22U 0402 10V6-K	PCIE_CRX_C_GTX_N3







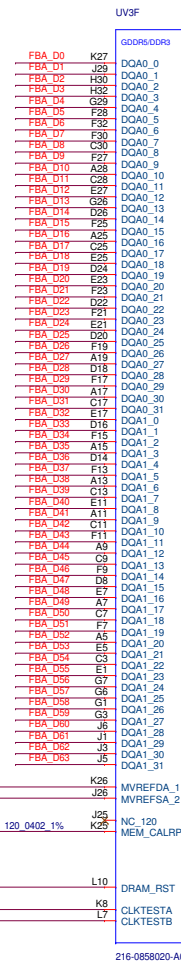
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ASIC Ball	Topaz	Jet
U10, T10 AB13, W9 AB11, AB12 AC11, AC13 AC14, Y9, W10	VDDC	NC
AC20	FB_VDDC	NC
AD20	FB_VSS	NC
W1	FB_VDDCI	NC
W3	FB_VSS	NC
AJ11	GPIO_SVC	NC_SVI2
AK12	GPIO_SVD	NC_SVI2
AL11	GPIO_SVT	NC_SVI2
N6	GPIO_11	NC_GPIO11
N5	GPIO_12	NC_GPIO12
N3	GPIO_13	NC_GPIO13
AJ27	WAKEB	NC_VSYNC
T8	PCC/GPIO_6	GPIO_6
AA3	PLL_ANALOG_OUT	NC
AA1	PLL_ANALOG_IN	NC

ASIC Ball	Topaz	Jet
U1	BP_0	NC
U3	BP_1	NC
AM26	DIECRACKMON	NC
Y11	NC	DBG_DATA13
AE9	NC	DBG_DATA14
L9	NC	DBG_DATA15
N9	NC	DBG_DATA16
AE8	NC	DBG_DATA12
AL9	NC	DBG_CNTL0
H13, H16, H19, J10 J23, J24, J9, K10 K23, K24, K9, L11 L12, L13, L20, L21 L22	VMEMIO	VDDR1
AA17, AA18 AB17, AB18	VDD_GPIO33	VDDR3
AA20, AA21 AB20, AB21	VDD_GPIO18	VDD_CT

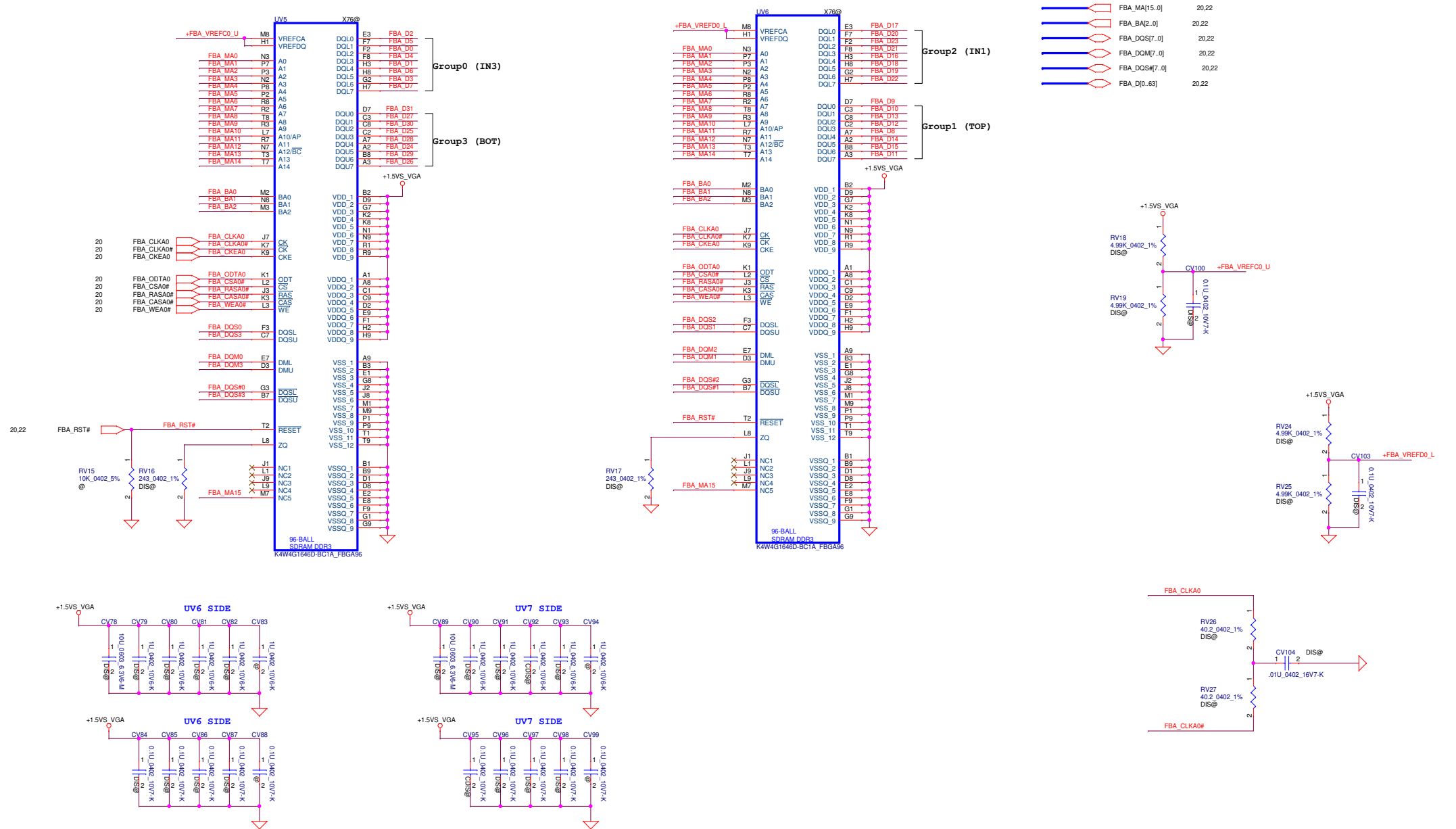
	Bits5	Bits4	Bits3	Bits2	Bits1
PS0	1	1	0	0	1
PS1	0	0	1	1	1
PS2	0	0	0	0	0
PS3	1	1	?	?	?




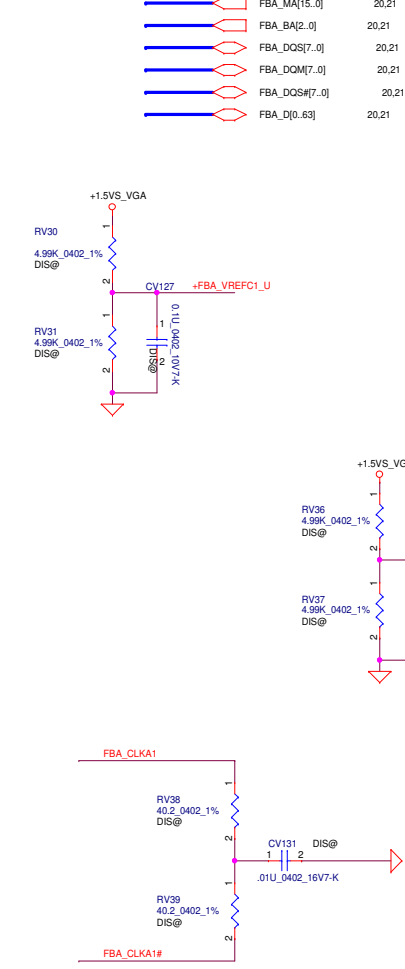
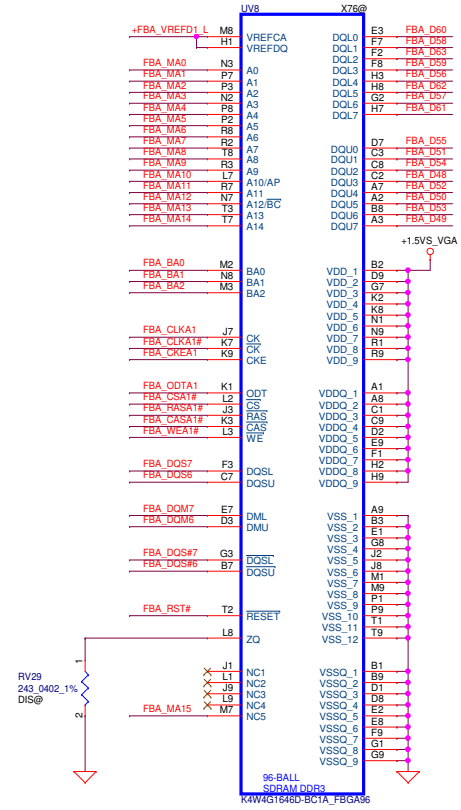
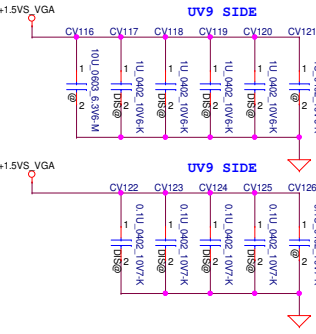
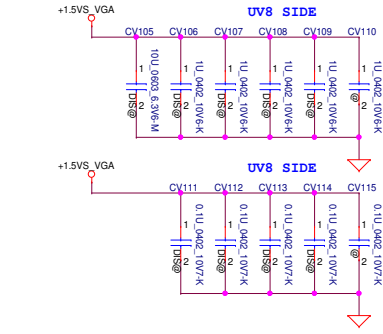
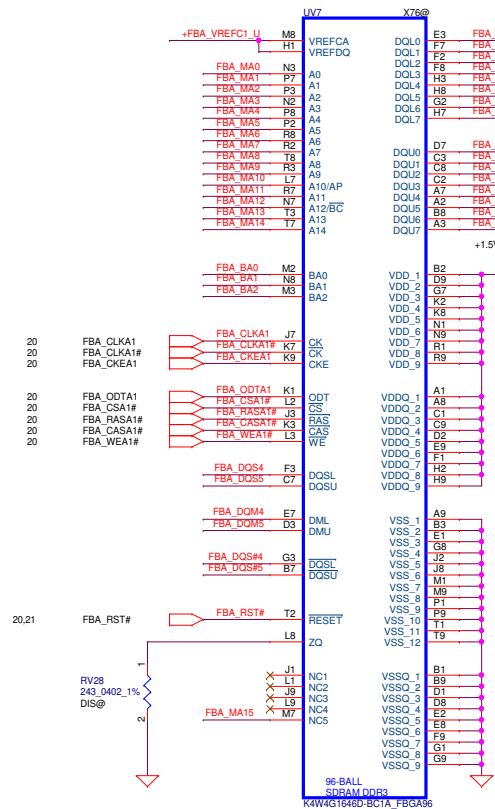
DIS®			
GD0R5/D0R3			
	K17	FBA MA0	
MAA0_0	J20	FBA MA1	
MAA0_1	H23	FBA MA2	
MAA0_2	G23	FBA MA3	
MAA0_3	G24	FBA MA4	
MAA0_4	H24	FBA MA5	
MAA0_5	J19	FBA MA6	
MAA0_6	K19	FBA MA7	
MAA0_7	G20	FBA MA15	
MAA0_8	L17	FBA MA15	
MAA0_9			
MAA1_0	J14	FBA MA8	
MAA1_1	K14	FBA MA9	
MAA1_2	J11	FBA MA10	
MAA1_3	J13	FBA MA11	
MAA1_4	H11	FBA MA12	
MAA1_5	G11	FBA BA2	
MAA1_6	J16	FBA BA0	
MAA1_7	L15	FBA BA0	
MAA1_8	G14	FBA MA14	
MAA1_9	K1		
WCKA0_0	E32	FBA DOM0	
WCKA0B_0	E30	FBA DOM1	
WCKA0_1	A21	FBA DOM2	
WCKA0B_1	G21	FBA DOM3	
WCKA1_0	E13	FBA DOM4	
WCKA1B_0	D12	FBA DOM5	
WCKA1_1	E3	FBA DOM6	
WCKA1B_1	F4	FBA DOM7	
	H28	FBA DOS0	
EDCA0_0	C27	FBA DOS1	
EDCA0_1	A23	FBA DOS2	
EDCA0_2	E19	FBA DOS3	
EDCA0_3	E16	FBA DOS4	
EDCA1_0	D10	FBA DOS5	
EDCA1_1	D6	FBA DOS6	
EDCA1_2	G5	FBA DOS7	
EDCA1_3			
	H27	FBA DOS8	
DBIA0_0	A27	FBA DOS9	
DBIA0_1	C23	FBA DOS2#	
DBIA0_2	C19	FBA DOS3#	
DBIA0_3	C15	FBA DOS4#	
DBIA1_0	E9	FBA DOS5#	
DBIA1_1	C5	FBA DOS6#	
DBIA1_2	H4	FBA DOS7#	
DBIA1_3			
ADBA0	L18	FBA ODTA0	FBA_ODTA0
ADBA1	K16	FBA ODTA1	FBA_ODTA1
CLKA0	H26	FBA CLKA0	FBA_CLKA0
CLKA0B	G25	FBA CLKA0#	FBA_CLKA0#
CLKA1	H9	FBA CLKA1	FBA_CLKA1
CLKA1B	G22	FBA CLKA1#	FBA_CLKA1#
RASA0B	H22	FBA RASA0#	FBA_RASA0#
RASA1B	G17	FBA RASA1#	FBA_RASA1#
CASA0B	G19	FBA CASA0#	FBA_CASA0#
CASA1B	G16	FBA CASA1#	FBA_CASA1#
CSA0B_0	H22	FBA CSA0#	FBA_CSA0#
CSA0B_1	J22		
CSA1B_0	K13	FBA CSA1#	FBA_CSA1#
CSA1B_1	K13		
CKEA0	K30	FBA CKEA0	FBA_CKEA0
CKEA1	J17	FBA CKEA1	FBA_CKEA1
WEA0B	G25	FBA WEA0#	FBA_WEA0#
WEA1B	H10	FBA WEA1#	FBA_WEA1#







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				Date:	Monday, August 01, 2016	Sheet 20 of 80 Rev 1.0


### Memory Partition A - Lower 32 bits

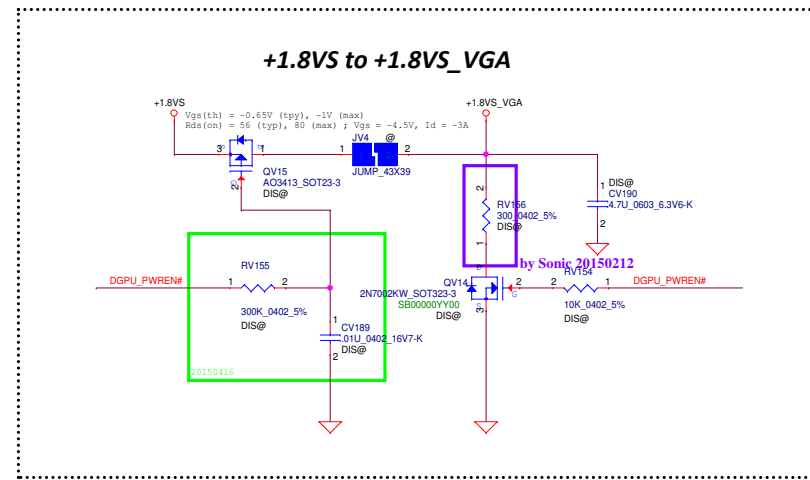
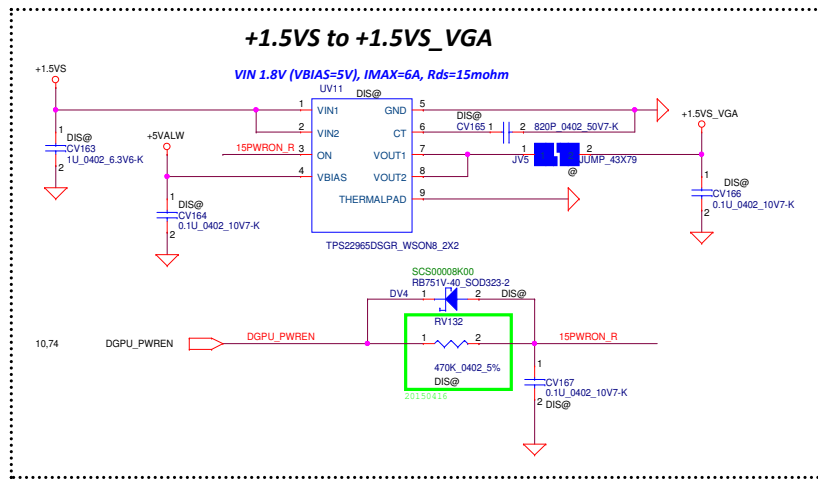


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Issued Date	2015/10/5	Deciphered Date	2014/09/07	Topaz & Jet DDR3 VRAM U		
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				Date:	Monday, August 01, 2016	Sheet 21 of 80 Rev 1.0

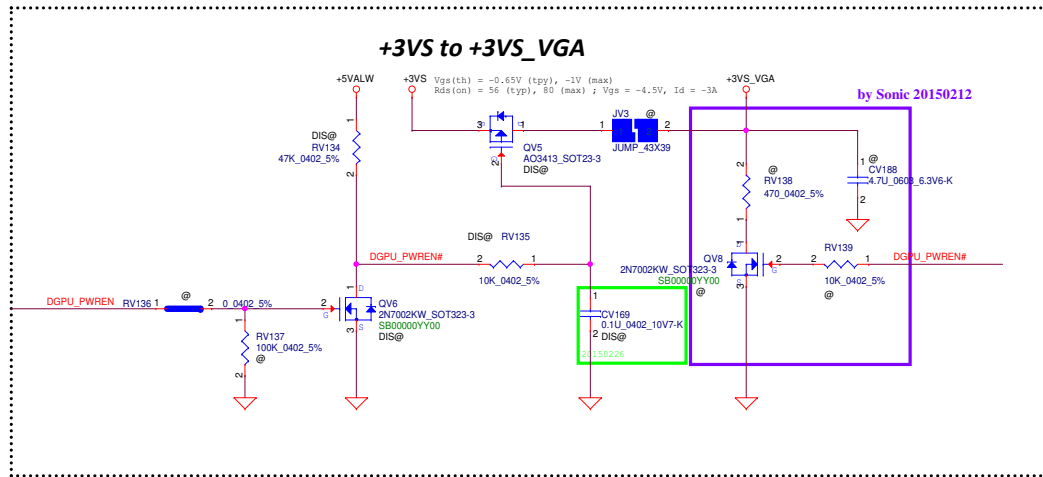
[illegible]

	FBA_MA[15..0]	20,21
	FBA_BA[2..0]	20,21
	FBA_DQS[7..0]	20,21
	FBA_DQM[7..0]	20,21
	FBA_DQS#[7..0]	20,21
	FBA_D[0..63]	20,21

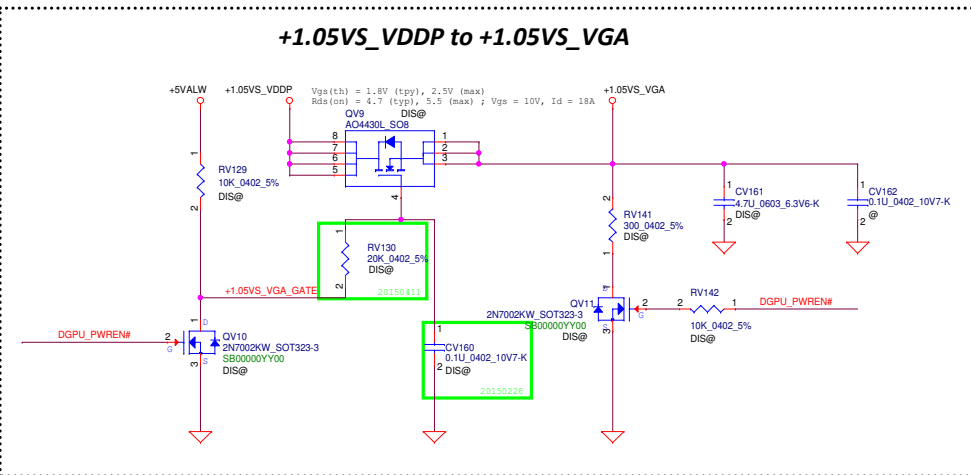
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Issued Date	2015/10/5	Deciphered Date	2014/09/07	Topaz & Jet DDR3 VRAM L			
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MLPS	Bit				
	5	4	3	2	1
PS_0[5:1]	1	1	0	0	1
PS_1[5:1]	1	1	0	0	0
PS_2[5:1]	1	1	0	0	0
PS_3[5:1]	1	1	X	X	X



PS_0[1]	ROM_CONFIG[0]	STRAP_BIOS_ROM_EN = 1 ROM_CONFIG[2:0] = [001] 256MB
PS_0[2]	ROM_CONFIG[1]	
PS_0[3]	ROM_CONFIG[2]	
PS_0[4]	N/A	1 (Default)
PS_0[5]	N/A	1 (Default)
PS_1[1]	STRAP_BIF_GEN3_EN_A	0 = PCIe GEN3 is not supported
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQB power management capability is disabled
PS_1[3]	N/A	0 (Default)
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	1 = The transmitter full-swing is enabled
PS_1[5]	STRAP_TX_DEEMPH_EN	1 = Tx deemphasis enabled
PS_2[1]	N/A	0 (Default)
PS_2[2]	N/A	0 (Default)
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device
PS_2[4]	N/A	1 (Default)
PS_2[5]	N/A	1 (Default)
PS_3[1]	BOARD_CONFIG[0]	PS_3[3..1] 101 = Micron 2G 110 = Samsung 2G 111 = Hynix 2G
PS_3[2]	BOARD_CONFIG[1]	
PS_3[3]	BOARD_CONFIG[2]	
PS_3[4]	N/A	1 (Default)
PS_3[5]	N/A	1 (Default)



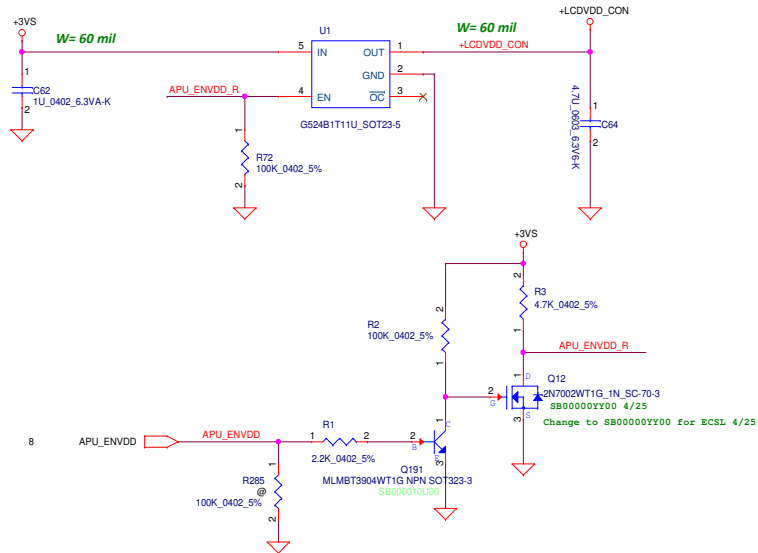
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Date: Monday, August 01, 2016				Sheet 24 of 80	

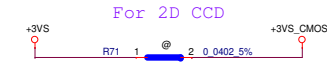




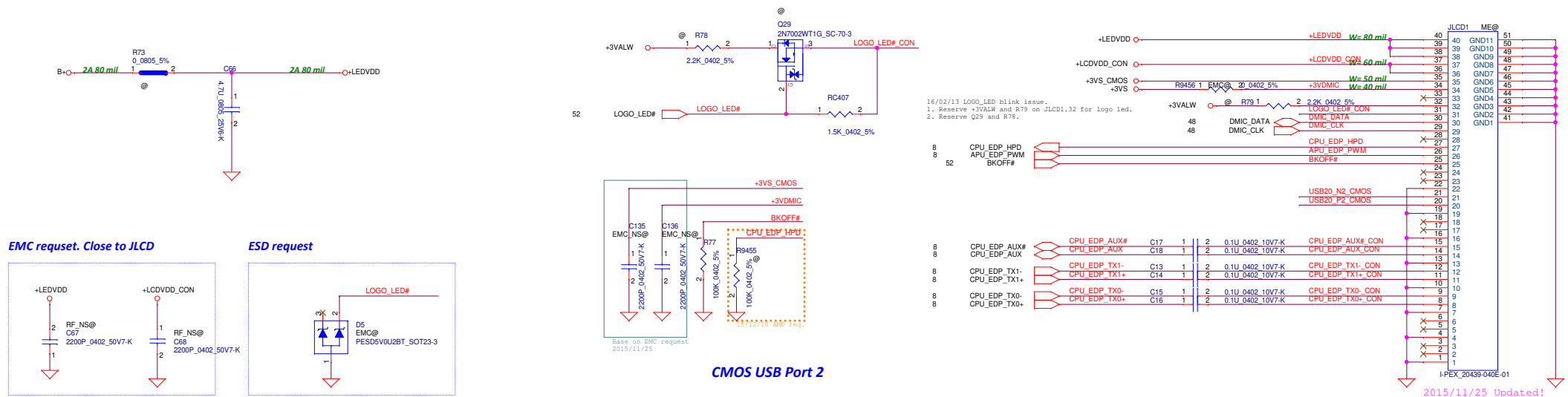
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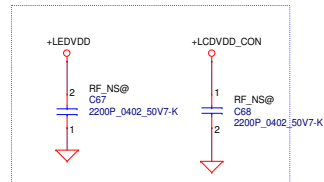
## CMOS Camera



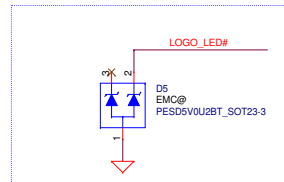
## eDP CONN.



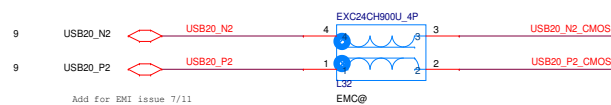
## EMC request. Close to JLCD



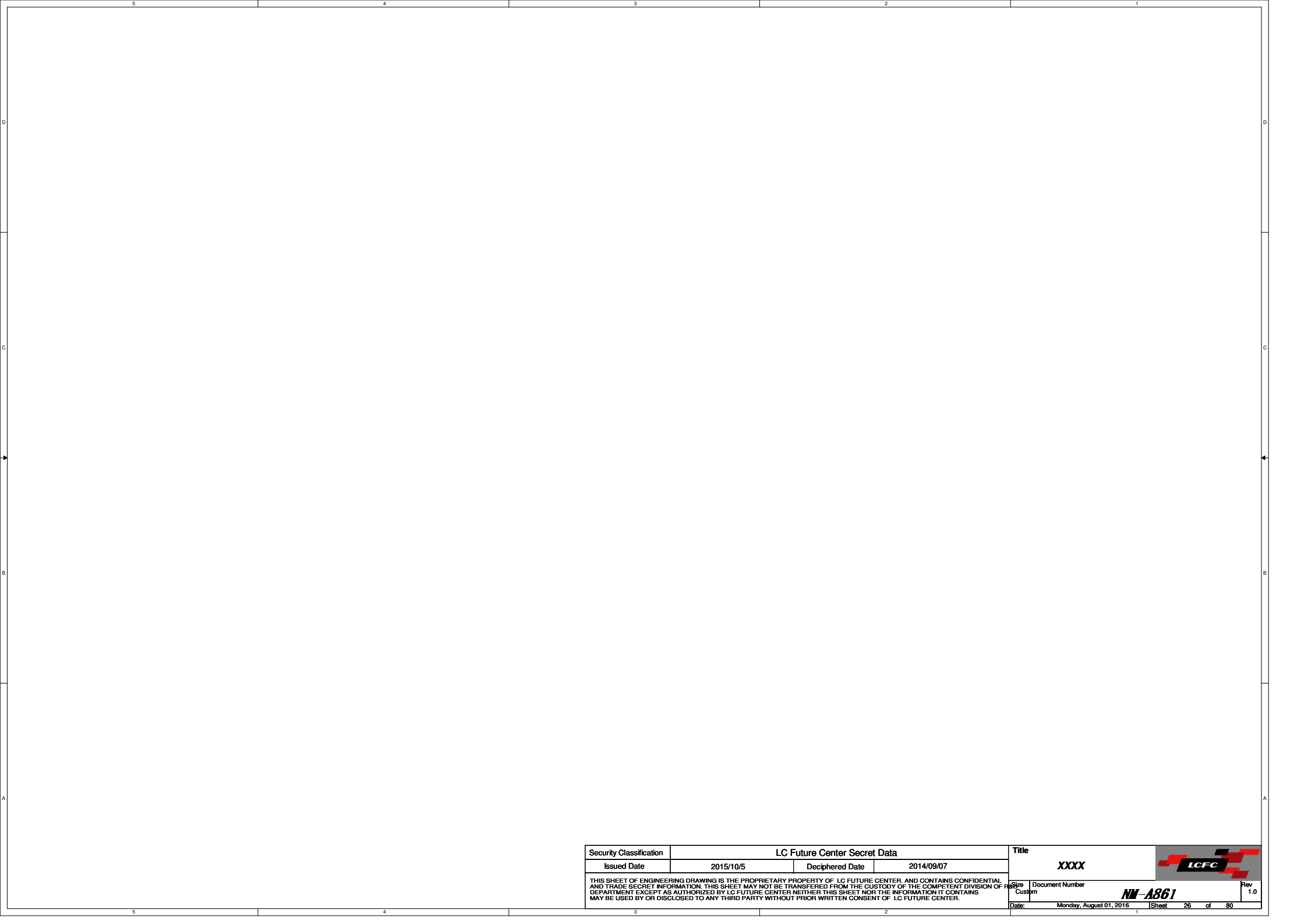
## ESD request





## CMOS USB Port 2




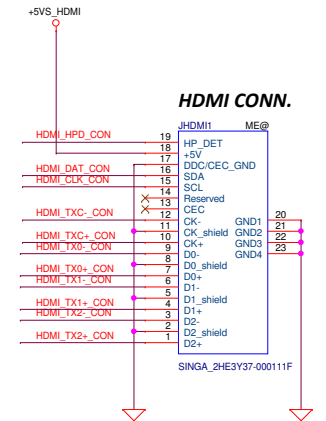
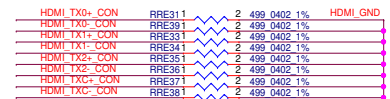
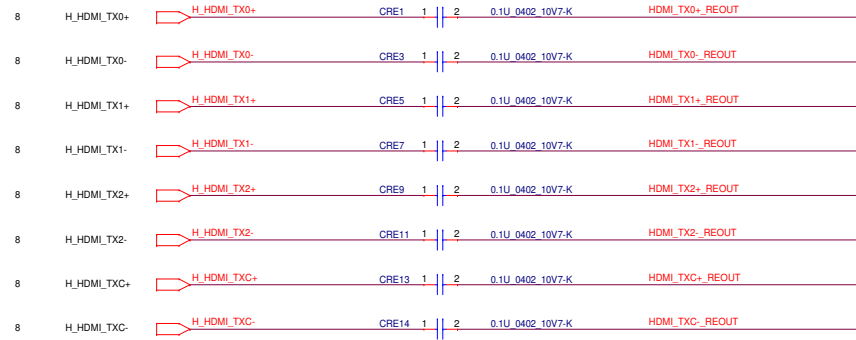
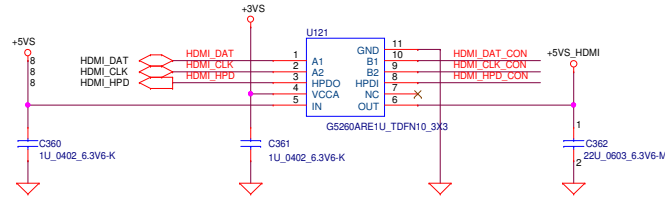
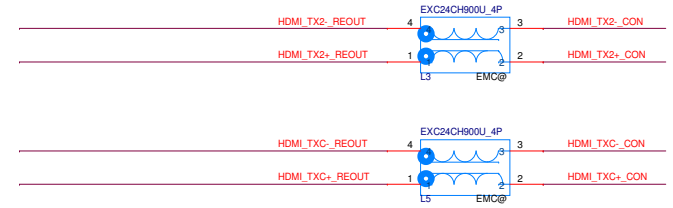
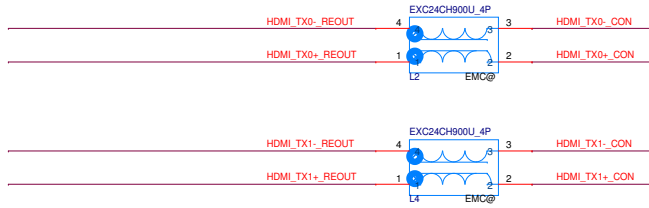
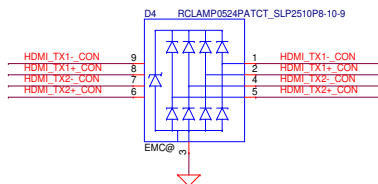
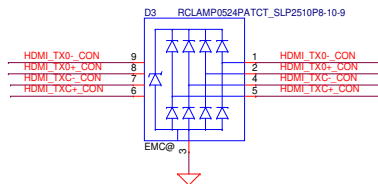
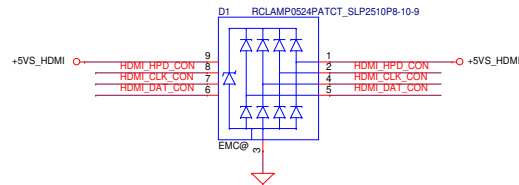
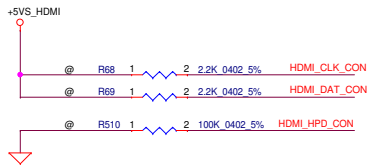
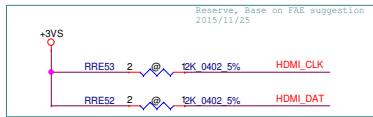
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Issued Date	2015/10/5	Deciphered Date	2016/12/31	eDP CONN	
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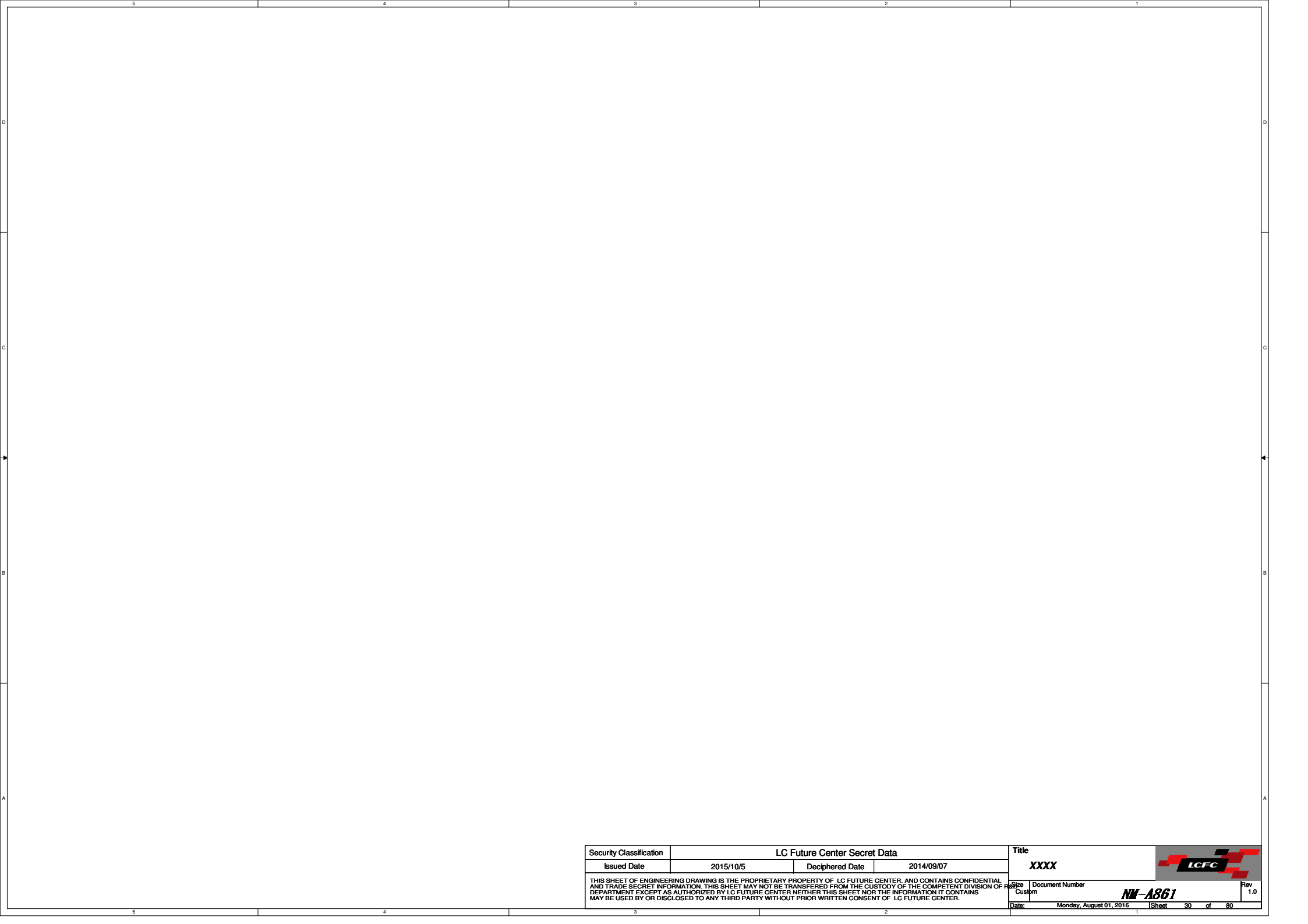
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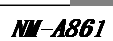
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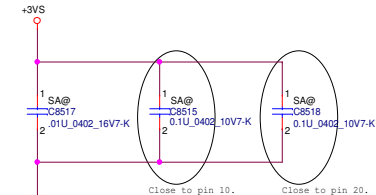
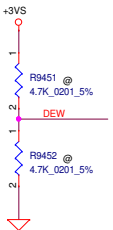
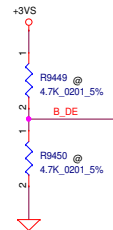
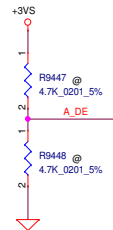
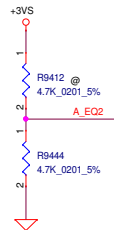
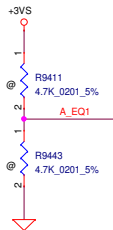
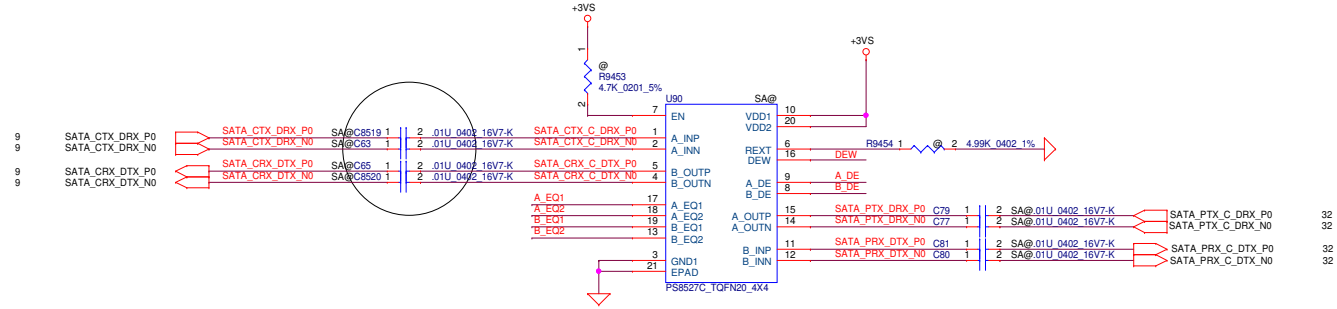


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SATA HDD Redriver



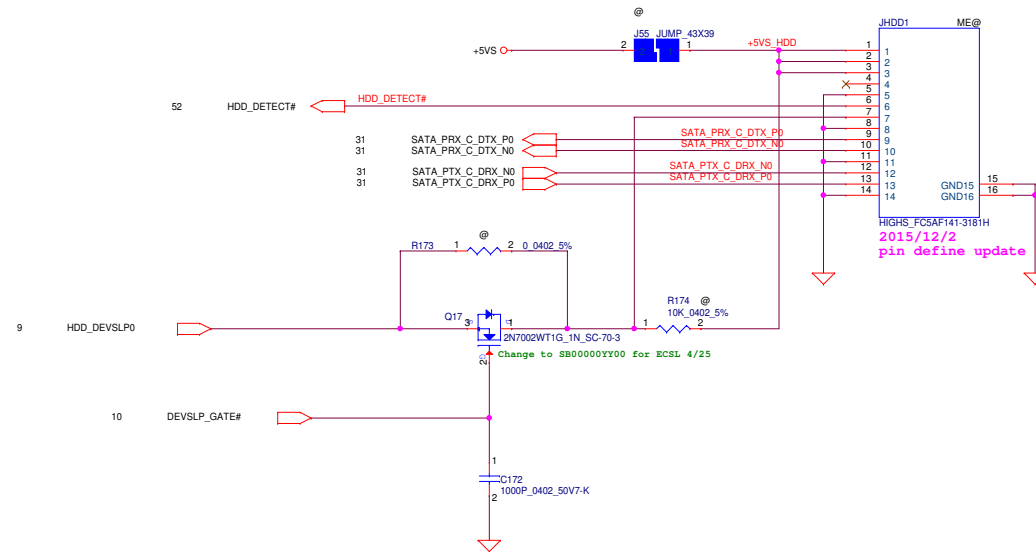
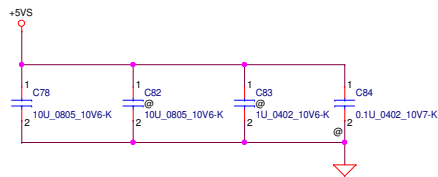
Change R9444, R9411, R9443 mount for SATA RX issue 4/21  
Delete R9411, R9443, add R9414 for SATA RX issue 7/4


Equalization level setting for Channel x(x=A/B),  
internally tied to VDD/2  
[x, EQ2, x, EQ2] ==  
L/M: for channel loss up to 2.4dB  
L/L: for channel loss up to 7.4dB  
L/R: for channel loss up to 14.4dB  
M/M: for channel loss up to 12.2dB (default)  
M/L: for channel loss up to 5.4dB  
M/R: for channel loss up to 13.3dB  
H/M: for channel loss up to 6.2dB  
H/L: for channel loss up to 11.2dB  
H/R: for channel loss up to 5dB

De-emphasis level setting for Channel x(x=A/B),  
internally tied to VDD/2  
[x, DE] ==  
M: -3.5dB (default)  
L: 0dB  
H: -6dB

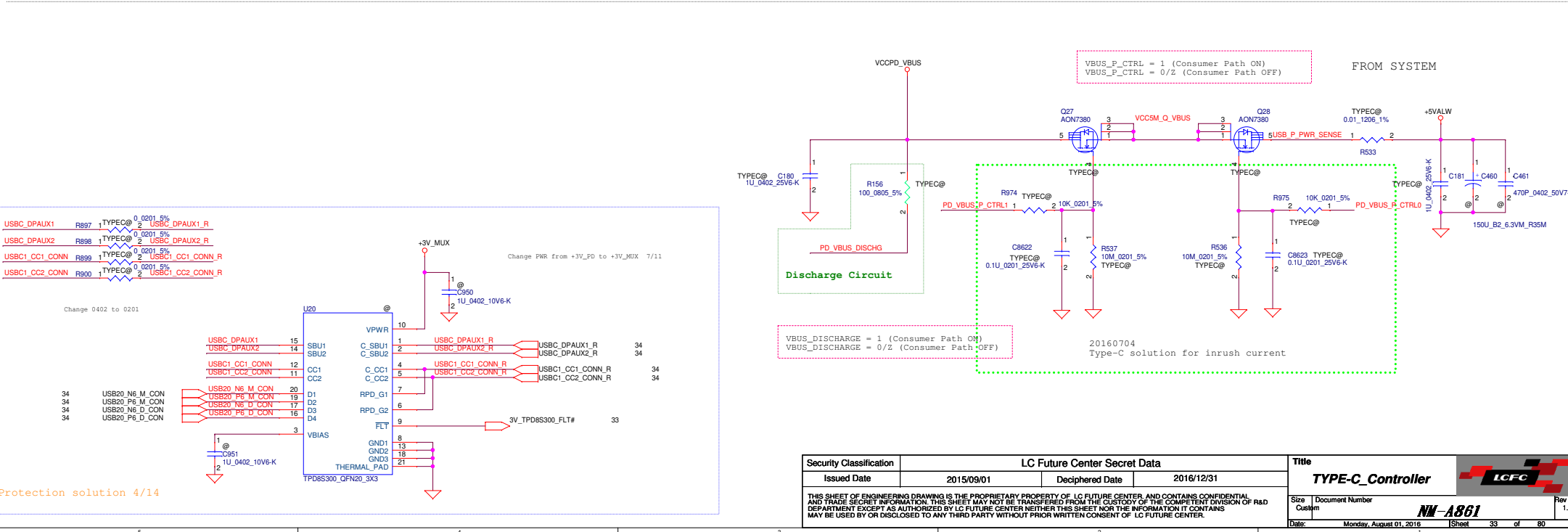
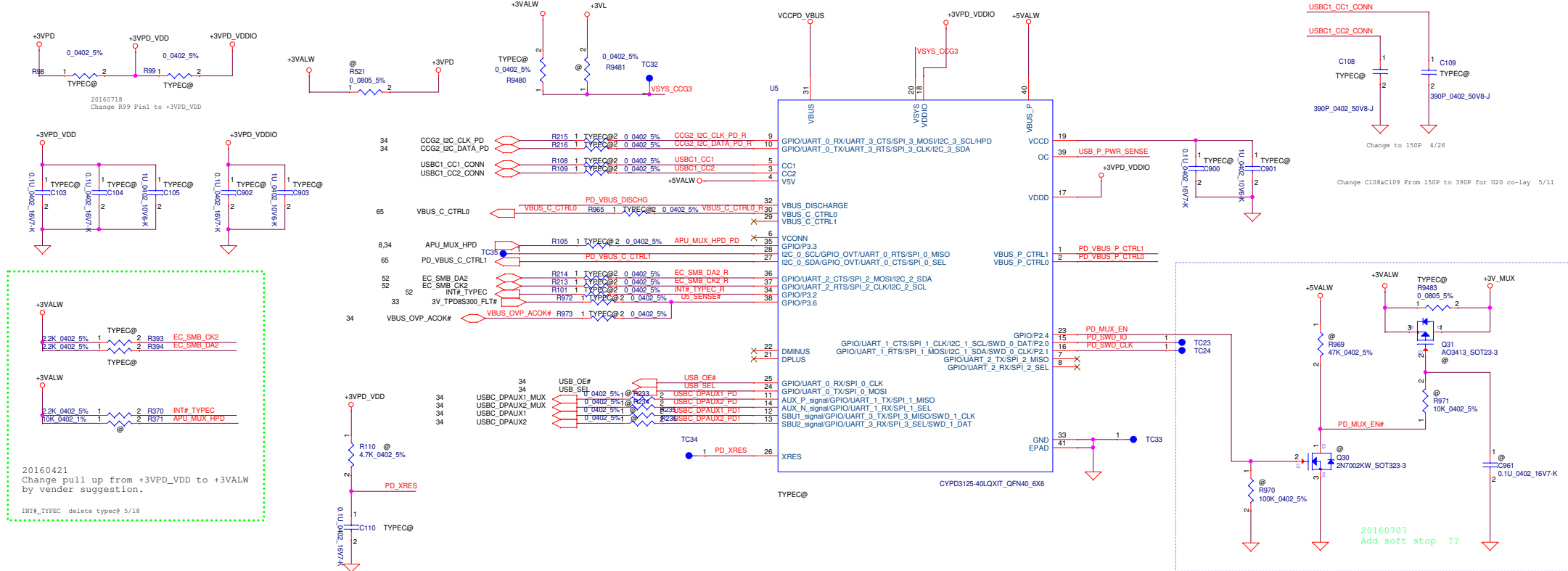
De-emphasis width adjustment,  
internally pulled down  
[DEW] ==  
M: for SATA3 (default)  
L: for SATA1  
H: for SATA2

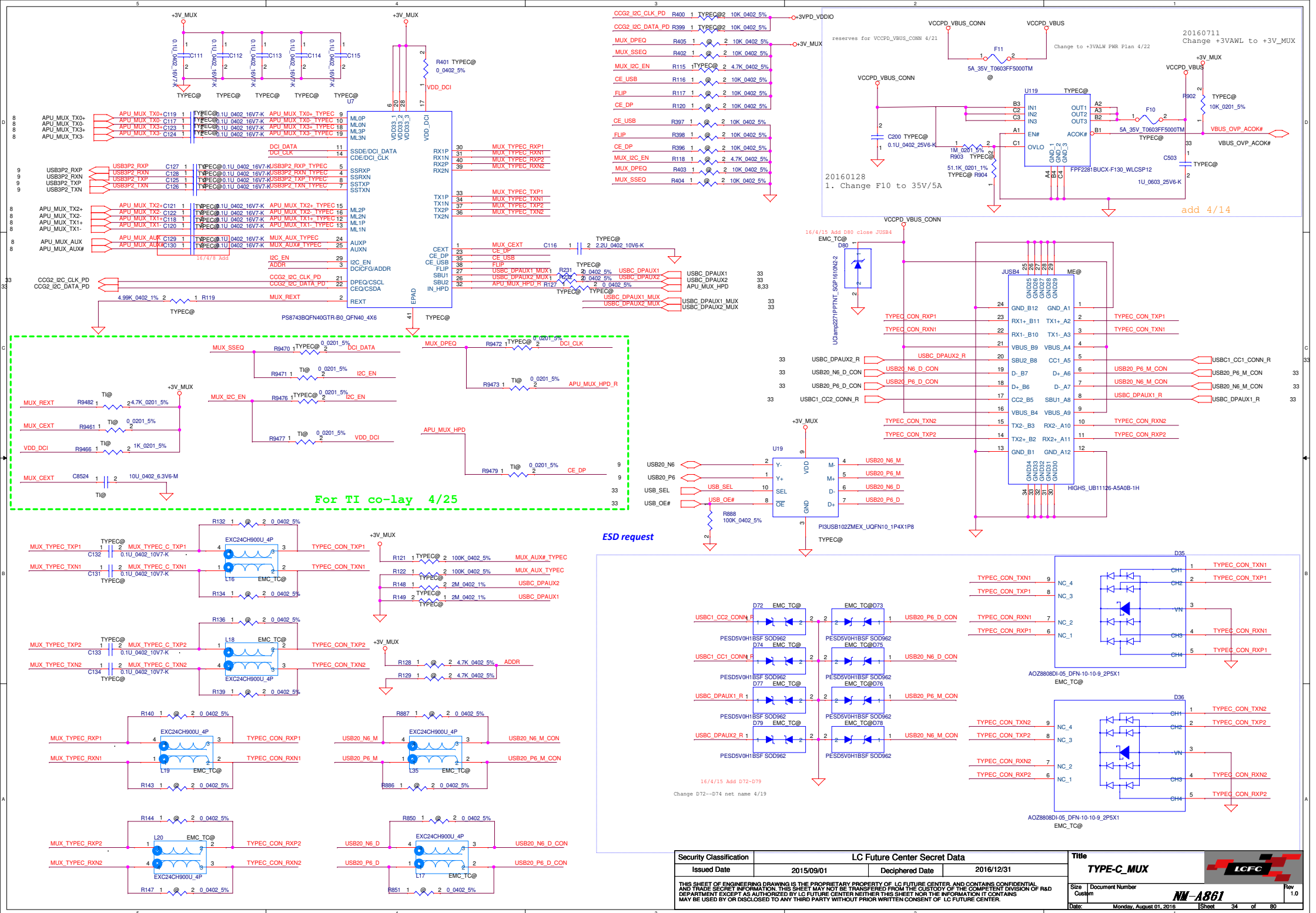
**SATA HDD CONN.**

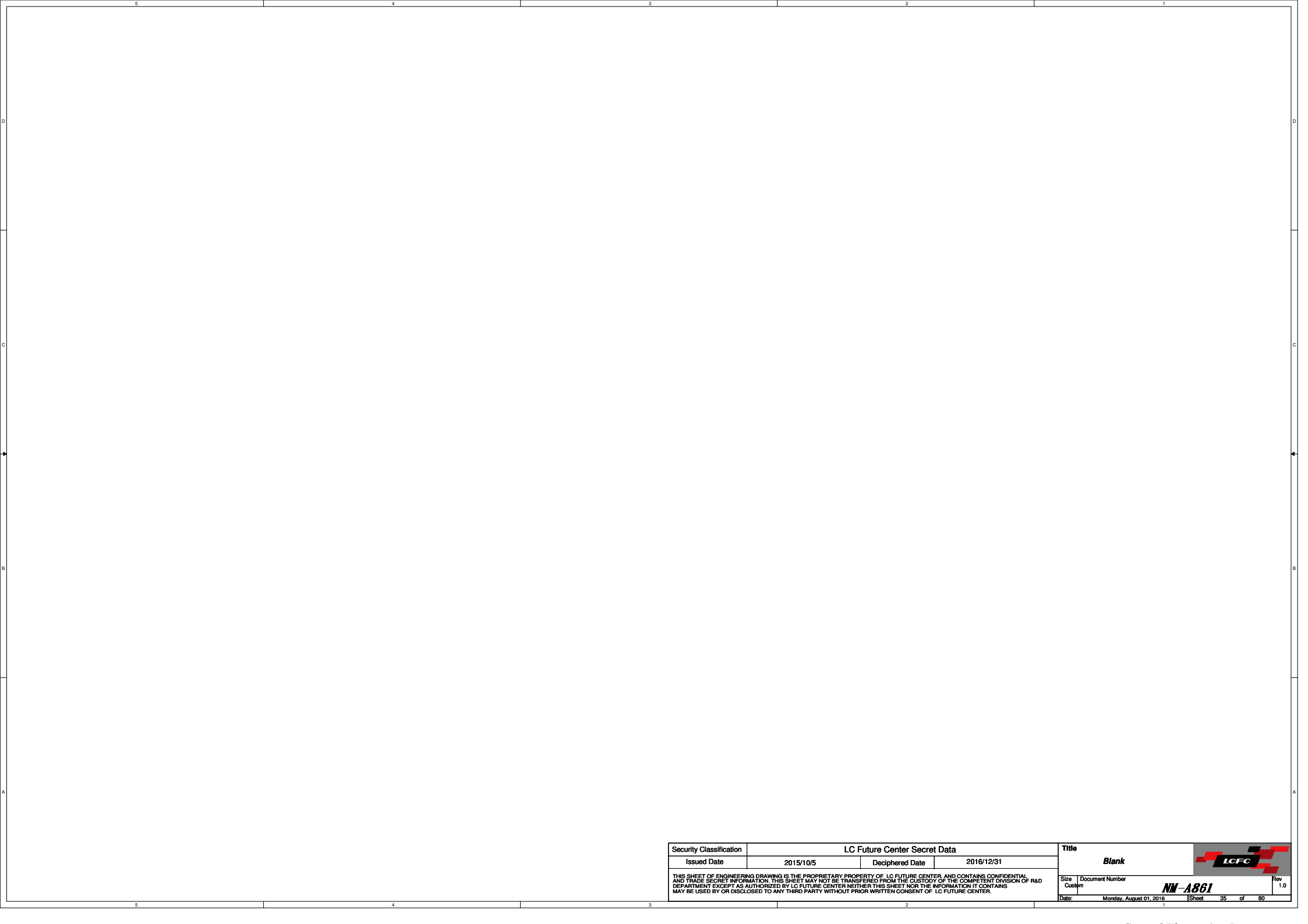


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Custom									
Date:				Monday, August 01, 2016		Sheet		32 of 80	








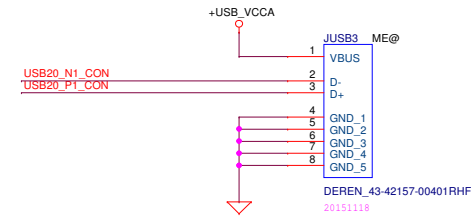
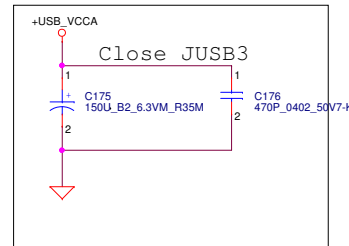
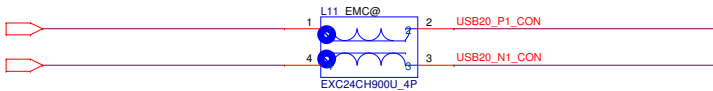
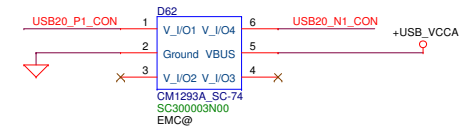
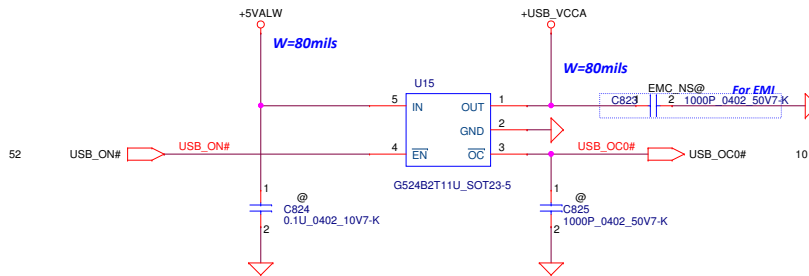


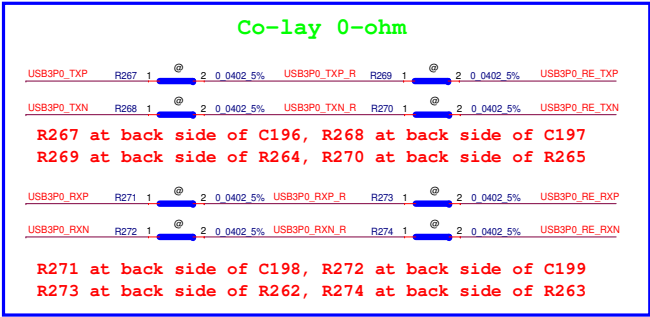
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				<small>Document Number</small> <b>NW-A861</b>	
<small>Date:</small> Monday, August 01, 2016				<small>Rev</small> 1.0	
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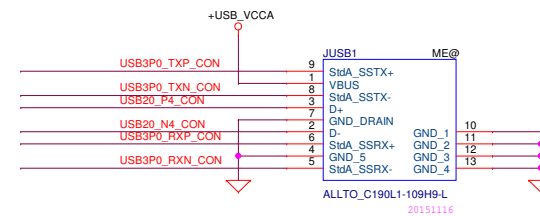
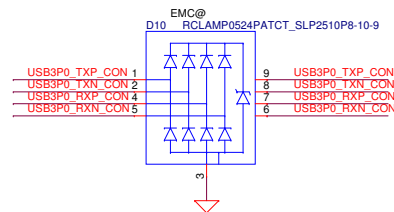
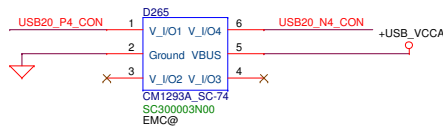
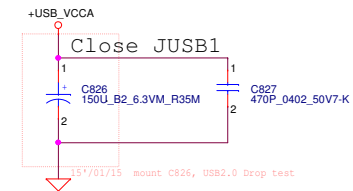
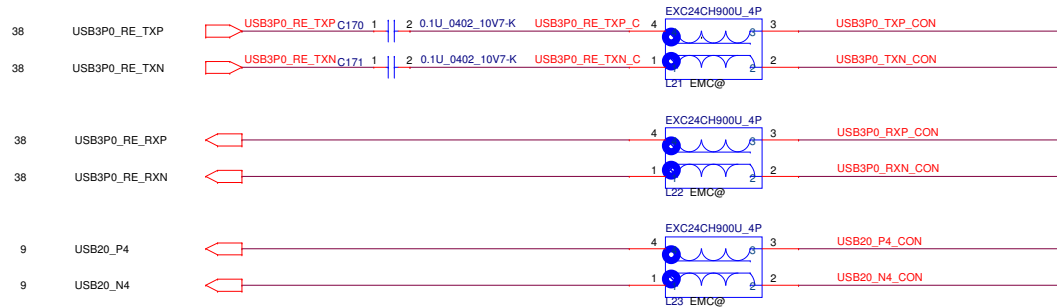
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				Custom	NW-A861	1.0
				Date:	Monday, August 01, 2016	Sheet 36 of 80

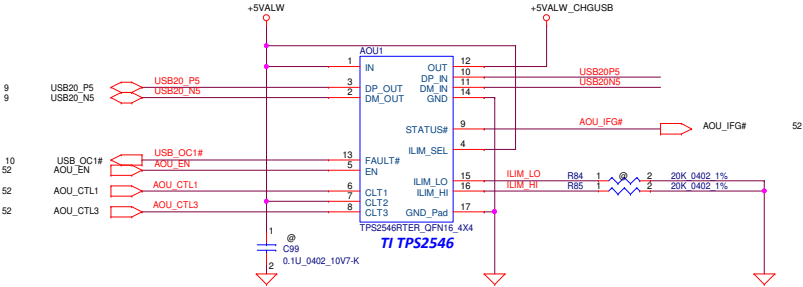




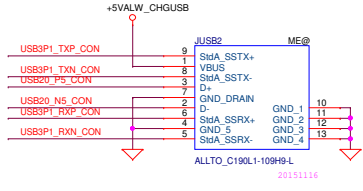
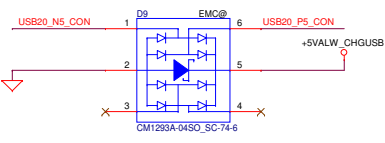
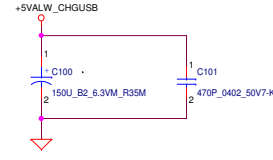
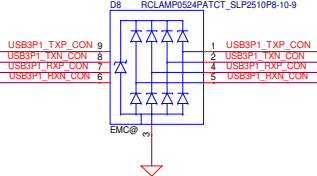
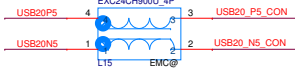
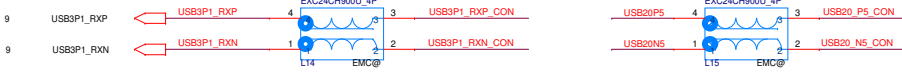
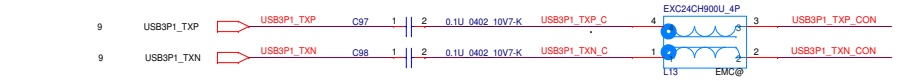
Security Classification	LC Future Center Secret Data			Title	
Issued Date	2015/10/5	Deciphered Date	2016/12/31	<b>USB Port2/3</b> Size C Custom	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Document Number <b>NW-A861</b>	Rev 1.0
				Date: Monday, August 01, 2016	Sheet 38 of 80



PORT1 (AOU)




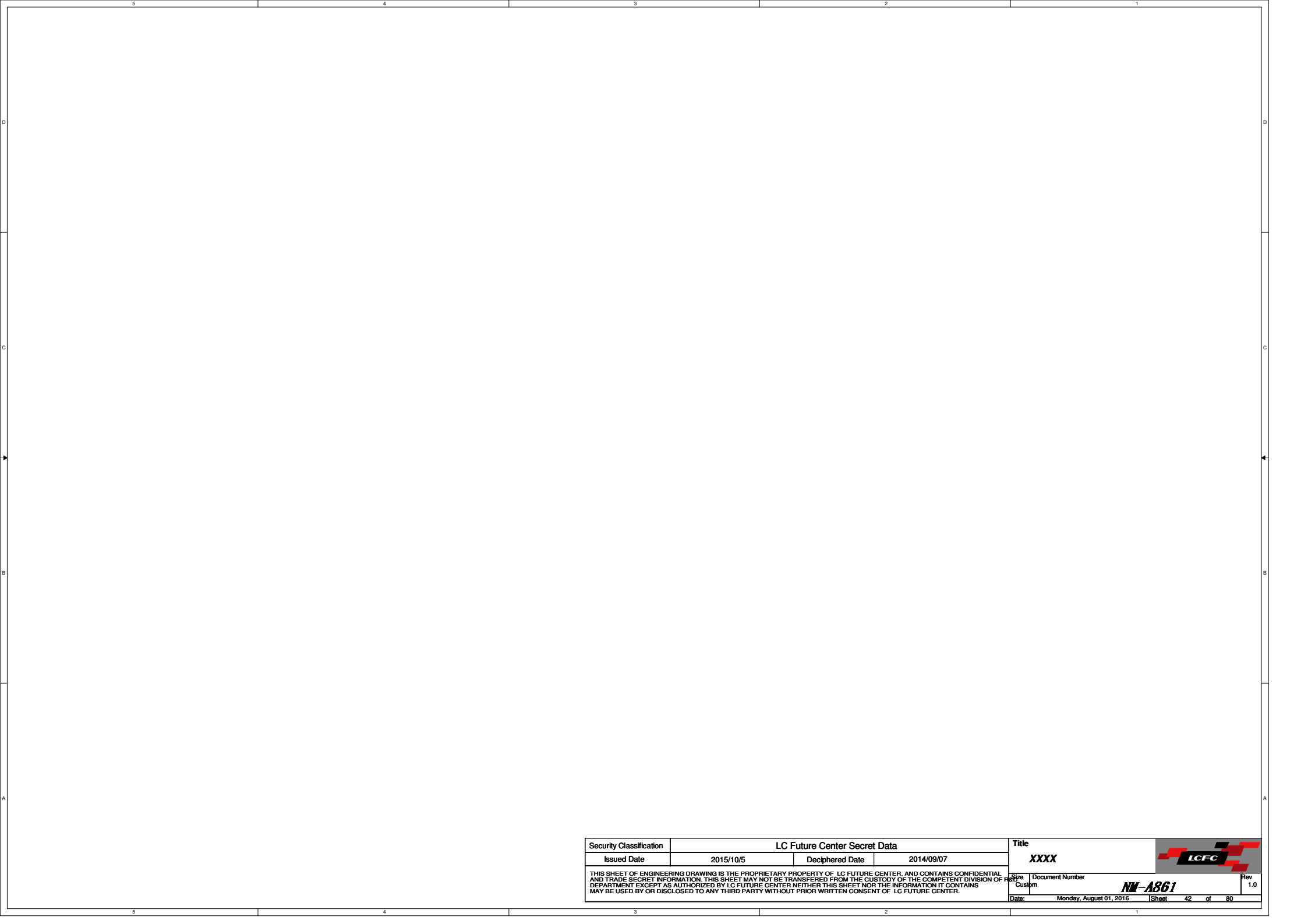
CLT1	CLT2	CLT3	ILIM_SEL	MOD
0	0	0	X	DCH OUT held low
1	1	1	1	CDP Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2 Data Connected
1	1	0	X	SDP1 Data Connected
0	1	0	X	SDP1 Data Connected
1	0	0	X	DCP_Short Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto Data Disconnected and Power Wake Function Active






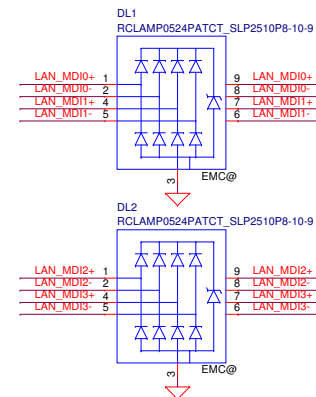
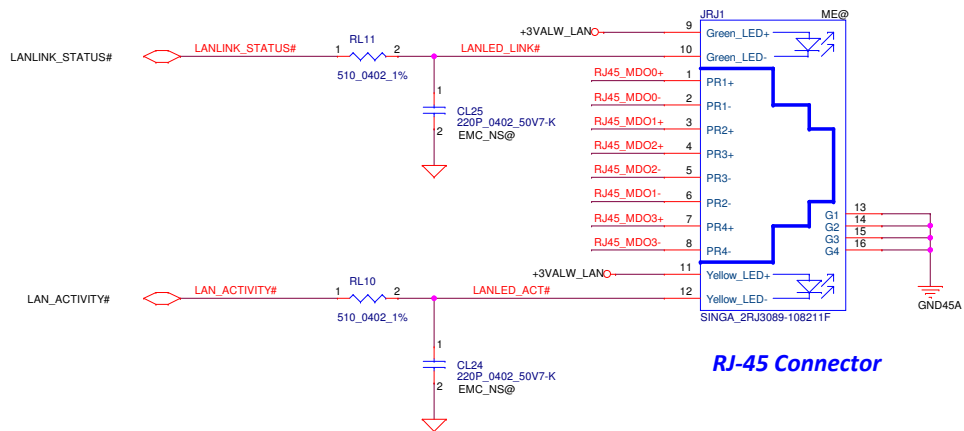
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Security Classification		LC Future Center Secret Data		Title		
Issued Date	2015/10/5	Deciphered Date	2014/09/07	DC V TO VS/ V-PCH/VM		
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				Date:	Monday, August 01, 2016	Sheet 41 of 80



Security Classification	LC Future Center Secret Data			Title	
Issued Date	2015/10/5	Deciphered Date	2014/09/07	XXXX	
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				Document Number	Rev
				<i>NW-A861</i>	1.0
				Date: Monday, August 01, 2016	Sheet 42 of 80

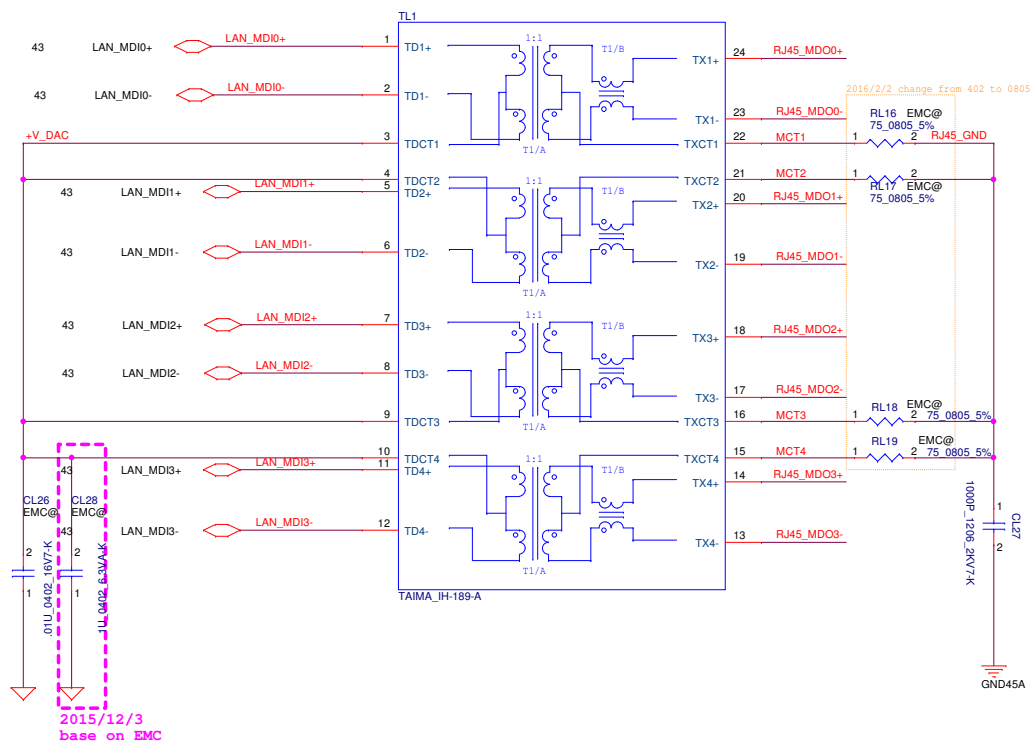






EMI

20150609

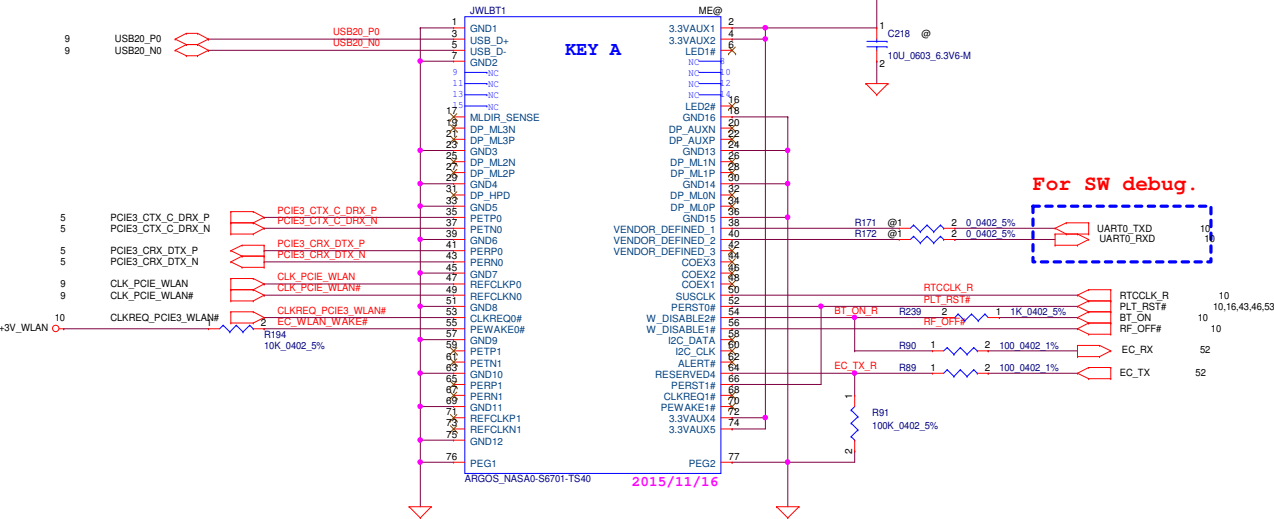
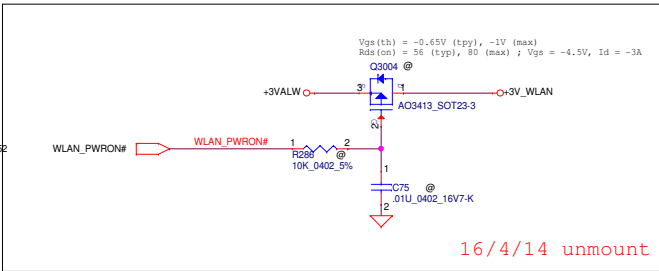
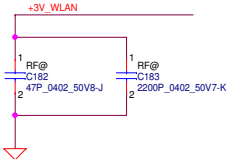
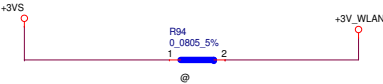
Reserve for Surge



Security Classification		LC Future Center Secret Data		Title			
Issued Date		2015/10/5		Deciphered Date			2014/09/07
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FPC DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.							
Size		Document Number		Custom		Rev	
Date:		Monday, August 01, 2016		Sheet		44 of 80	


TYPE-A NGFF CCARD FOR WLAN

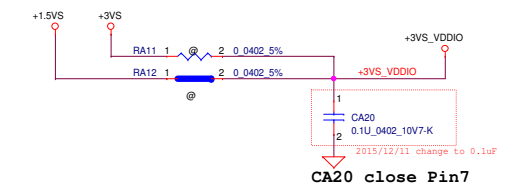
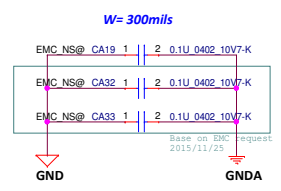
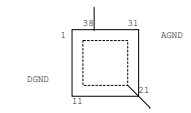
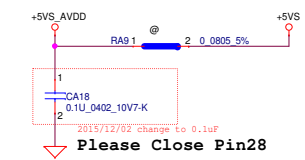
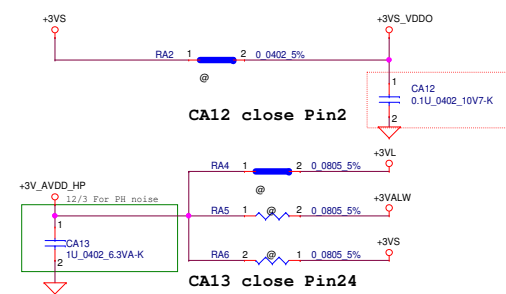
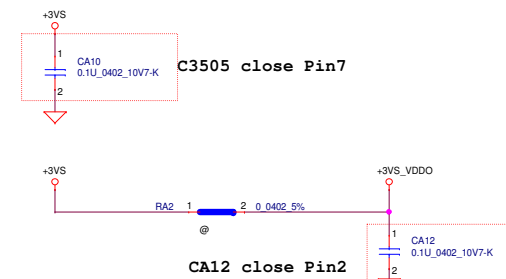
3.2H CONNECTOR






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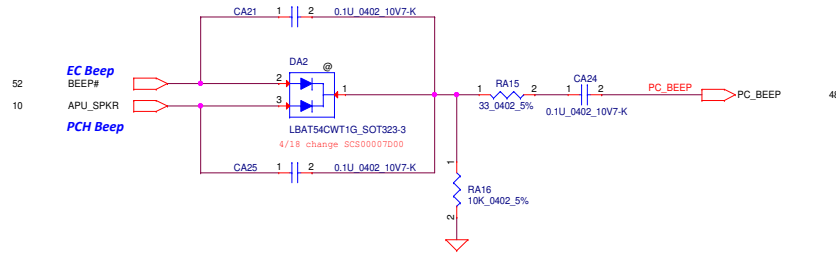
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Issued Date	2015/10/5	Deciphered Date	2016/12/31	BLANK			
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				Custom		NW A861	1.0
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Security Classification		LC Future Center Secret Data		Title		
Issued Date	2015/10/5	Deciphered Date	2016/12/31	Audio Codec		
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				Date:	Monday, August 01, 2016	Sheet 48 of 80 Rev 1.0

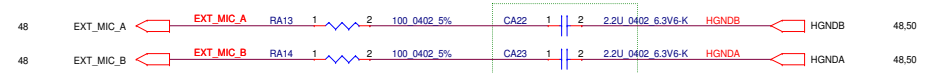


## PC BEEP



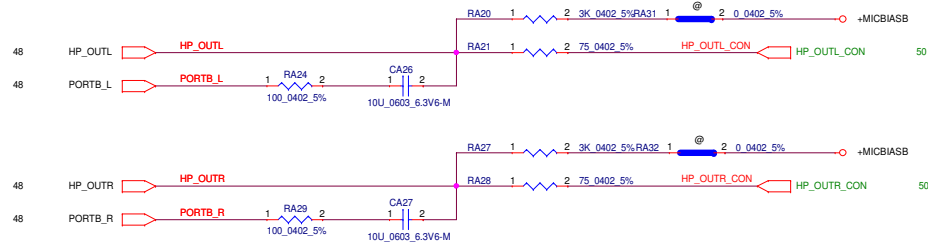
## EXT. MIC/LINE IN

Apple --> EXT\_MIC\_A, HGND B  
Nokia --> EXT\_MIC\_B, HGND A

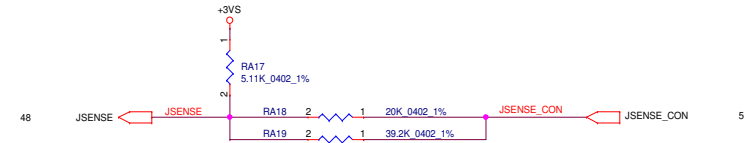


Changed CA29 & CA30 from 1uF to 2.2uF/X5R to meet Port-D(headset-Mic) THD+N <= -65 dB

## HeadPhone/LINE OUT

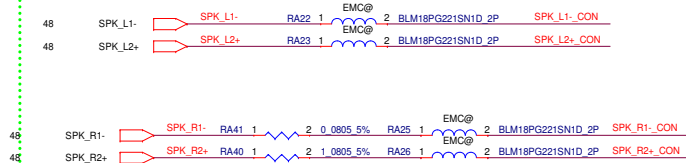


CA31, CA32 change to 4.7uF for Quality requirement



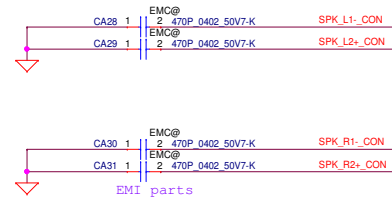
## Speaker OUT

Need Length Match

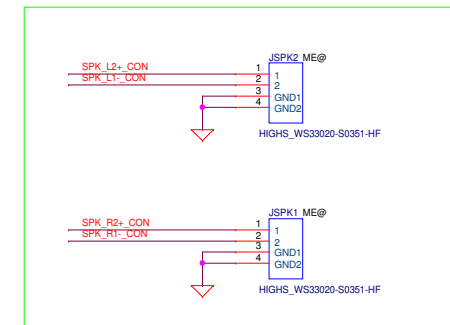


16/4/8 change RA40, RA41 to 1ohm, 0ohm for speaker gain balance fine tune.

Change RA40 to SD00001XY0T 4/25

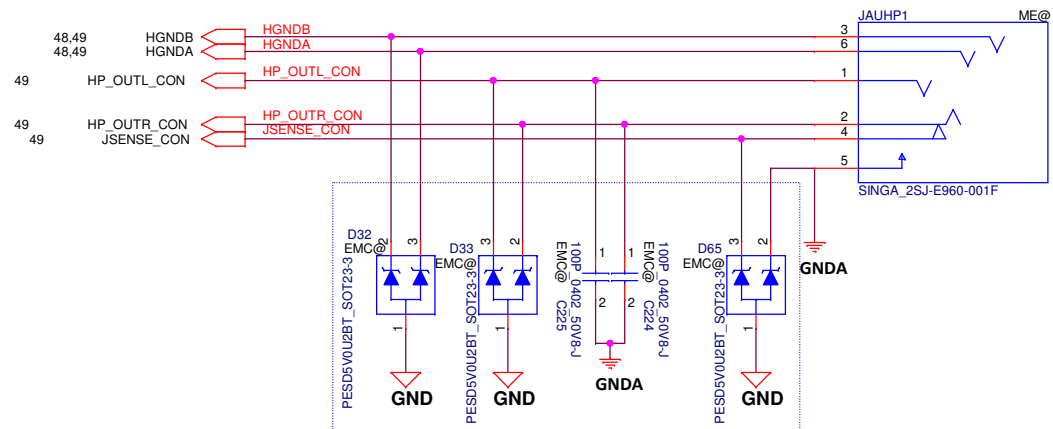


## SPK CONN.




2015/11/13 check pin1, 2 again!!

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/10/5	Deciphered Date	2016/12/31	HP/MIC JACK/Speaker	
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				Customer	NW-A861
				Date	Monday, August 01, 2016
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				Rev	1.0




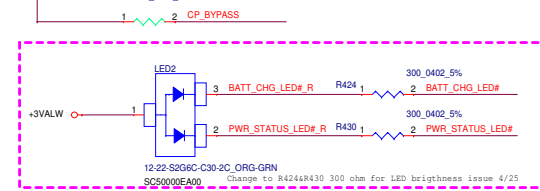
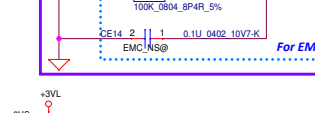
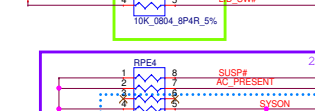
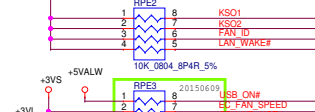
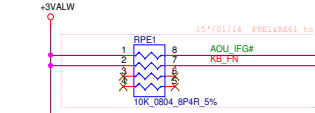
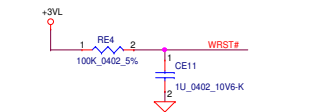
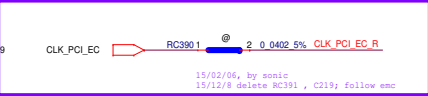
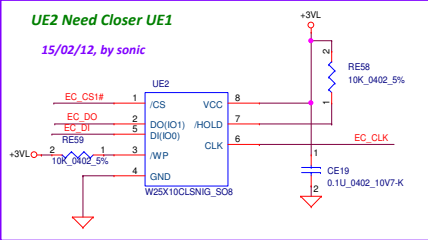
Vendor suggestion.  
Reserve for EMI.  
Close to JAUHP.

Security Classification		LC Future Center Secret Data		Title					
Issued Date	2015/10/5	Deciphered Date	2016/12/31	AUDIO JACK					
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						Date:	Monday, August 01, 2016		
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NM-A861

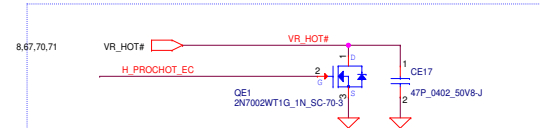
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Issued Date		2015/10/5	Deciphered Date	2016/12/31	BLANK	
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&amp;D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</small>						
Size	Document Number				Rev	
Custom	NW-A861				1.0	
Date: Monday, August 01, 2016					Sheet 51 of 80	



16/02/13 Chagne LED2 symbol and swap BATT\_CHG\_LED# & PWR\_STATUS\_LED#

**PROCHOT#**  
(EC asserts PROCHOT# signal by driving high, the level shifter must invert it and drive the processor side PROCHOT# low.)



8.67,70,71

VR\_HOT#

H\_PROCHOT\_EC

OE1 2N7002WT1G\_1N\_SC-70-3

CE17 47P\_0402\_50V8-J

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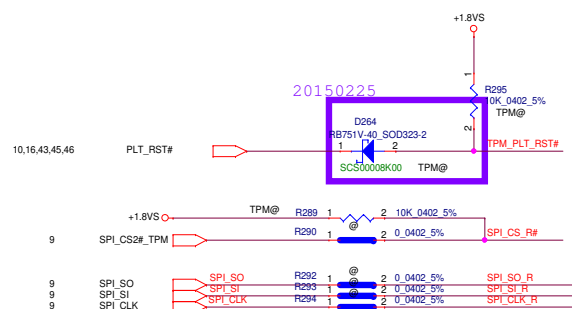
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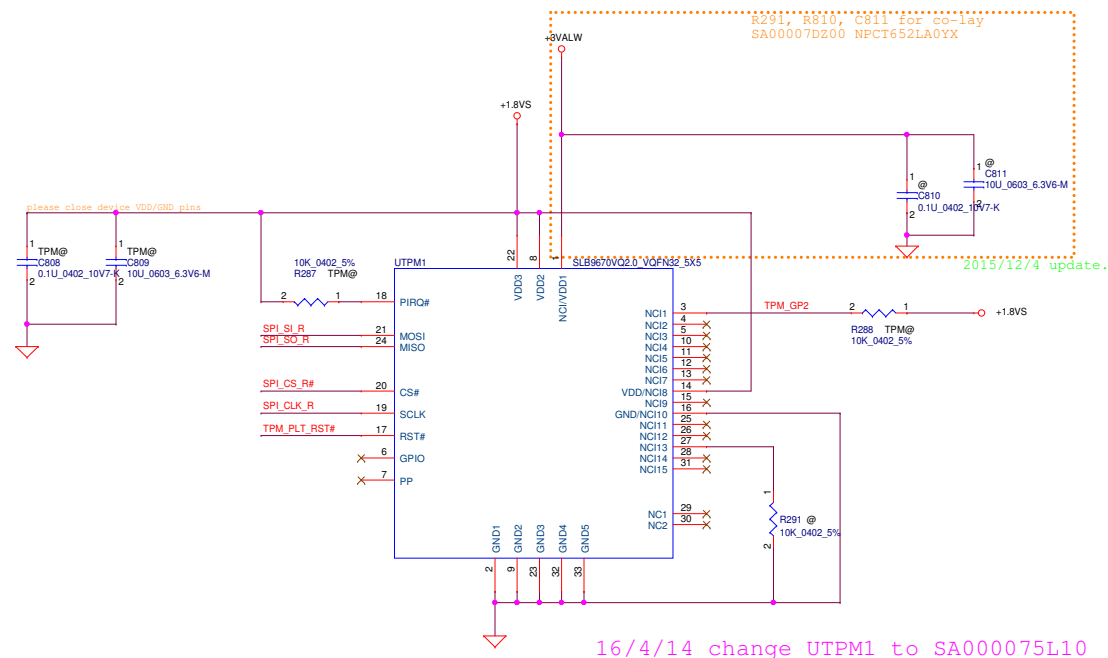
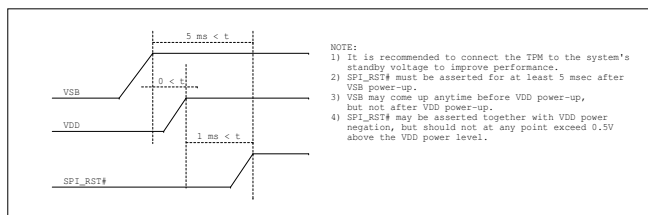
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293

Only for UMA SKU

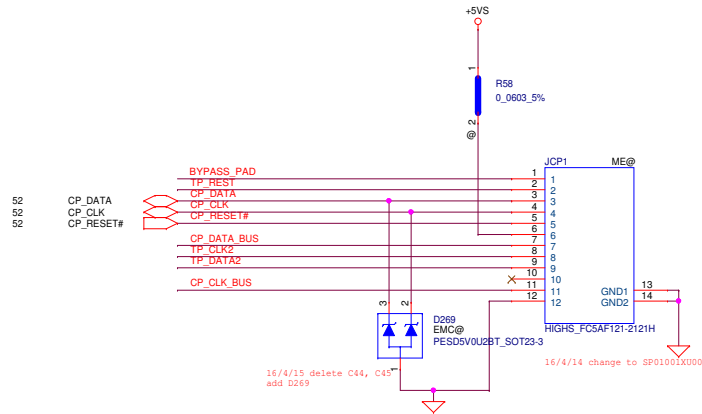


NOTE:  
Check timing sequence in SDV phase.

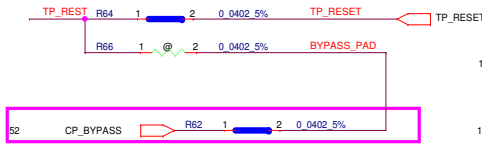
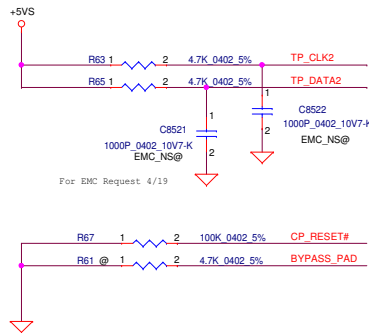
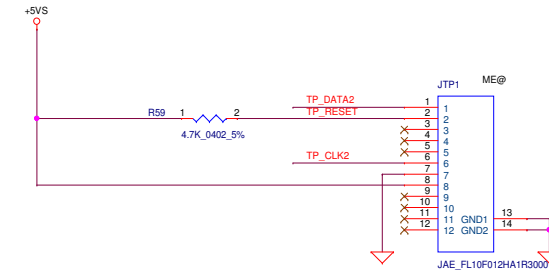


Security Classification				LC Future Center Secret Data				Title		
Issued Date		2015/10/5		Deciphered Date		2016/12/31		TPM		
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								Document Number <b>NW-A861</b>		Rev 1.1
Date:								Monday, August 01, 2016		Sheet 53 of 80

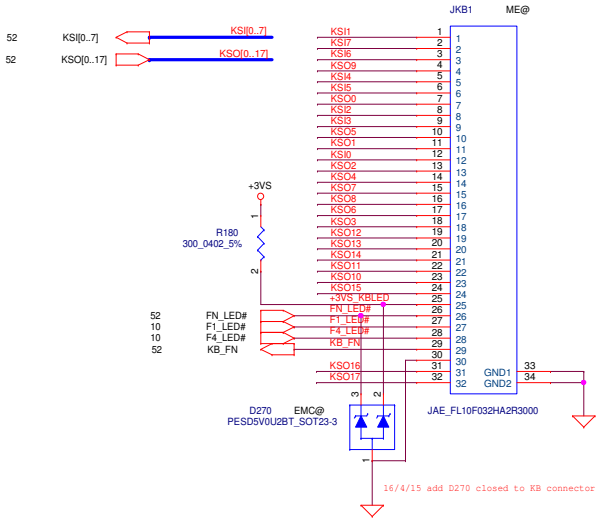
Click Pad



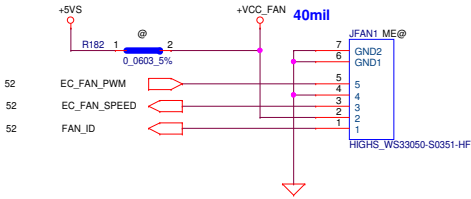
Track point



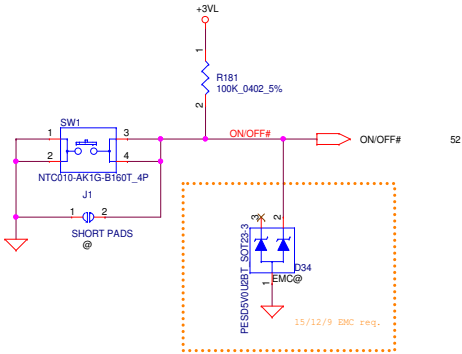
KB CONN



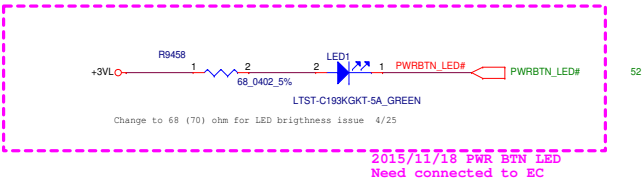
FAN CONN.



PWR BTN

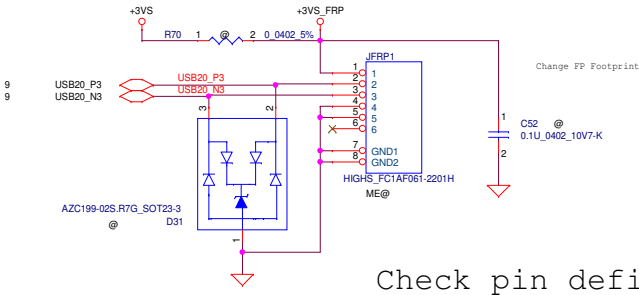


LED

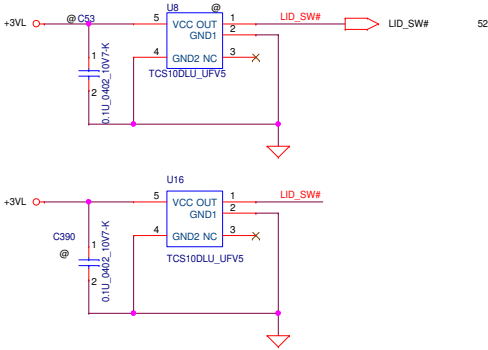


FingerPrint CONN.

15/12/18 delete finger printer function  
make all FRP circuit to "0" and will be delete at next version.

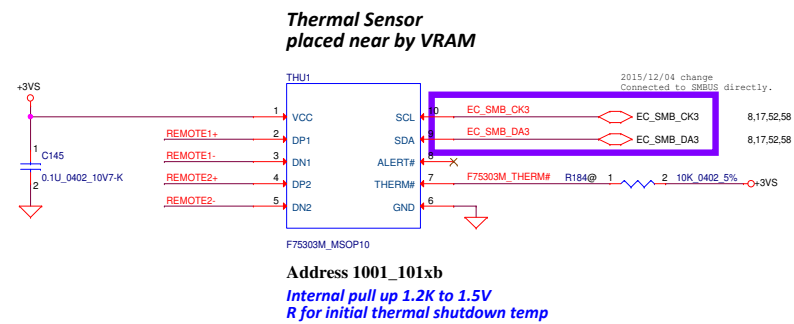


Lid Switch

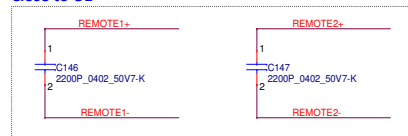


16/02/13  
1. Co-lay U16 & U18  
2. Co-lay U8 & U19

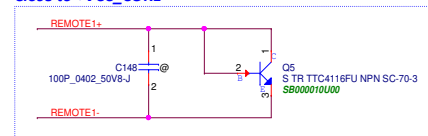




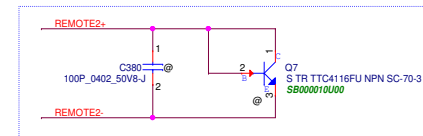
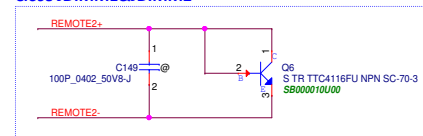
**Close to U1**



**Close to +VCC\_CORE**

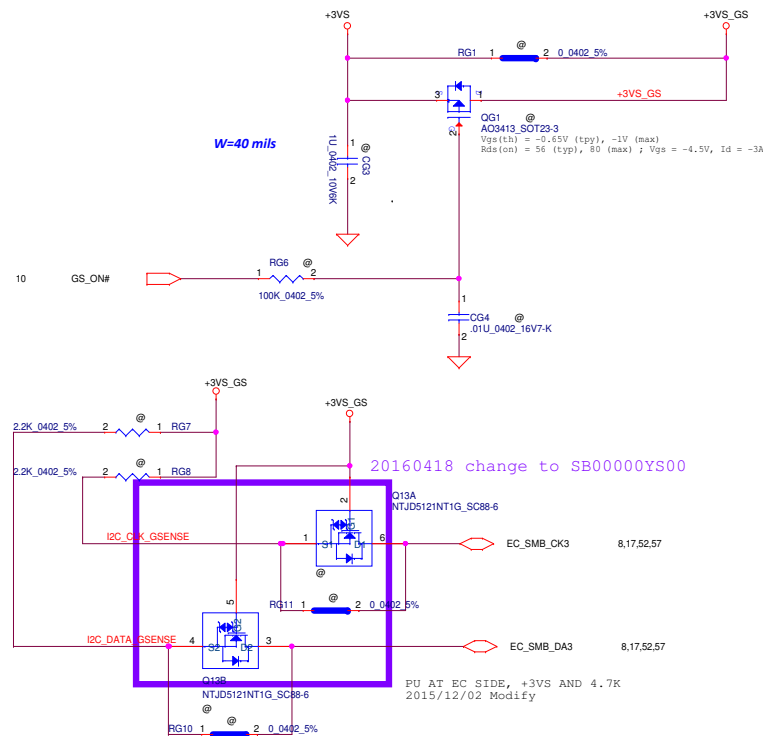


**Close JDIMM1&JDIMM2**

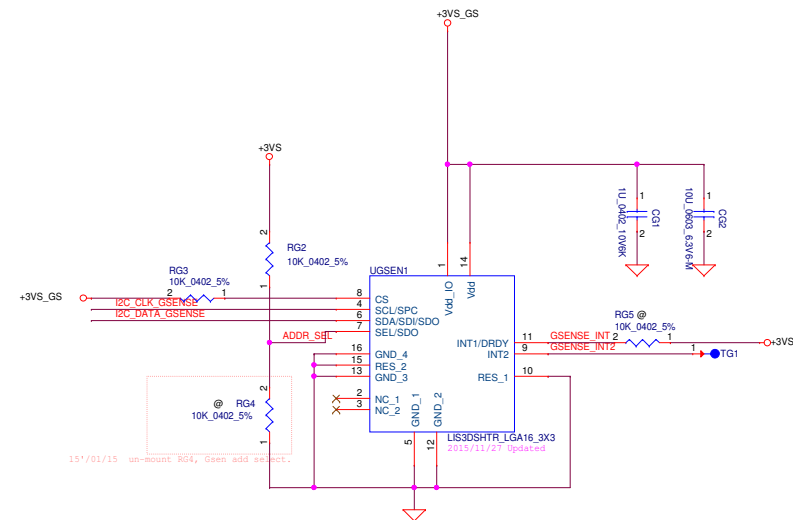


**REMOTE2+/-:**  
Trace width/space:10/10 mil  
Trace length:<8"

Security Classification	LC Future Center Secret Data			Title	
Issued Date	2015/10/5	Deciphered Date	2016/12/31	Thermal Sensor	
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## APS G-Sensor






TABLE

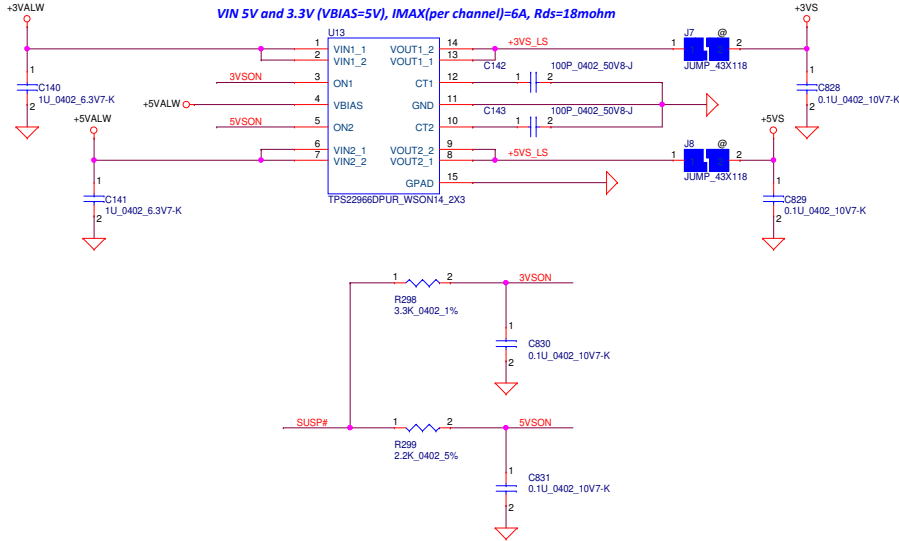
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LIS3DH	H L	32h (W) & 33h (R) 30h (W) & 31h (R)
KX023-1025	H L	3Eh (W) & 3Fh (R) 3Ch (W) & 3Dh (R)

TABLE

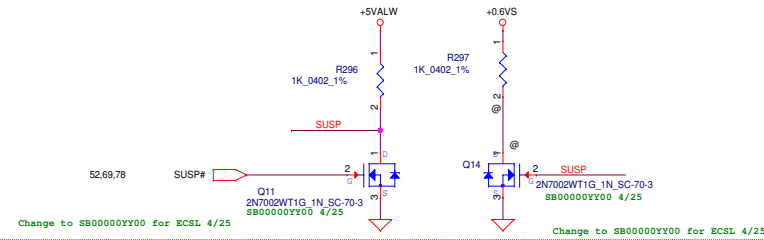
P/N	Mode Selection
H	I2C Mode
L	SPI Mode

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D				D																												
C				C																												
B				B																												
A				A																												
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Issued Date	2015/10/5	Deciphered Date	2014/09/07	XXXX																												
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Date:		Monday, August 01, 2016		Sheet	59	of	80																									
5	4	3	2	1																												

**+5VALW To +5VS**  
**+3VALW To +3VS**

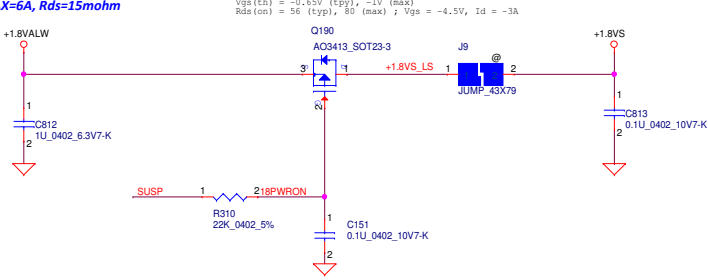


**For DisCharge**



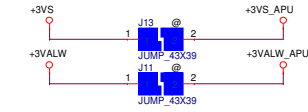
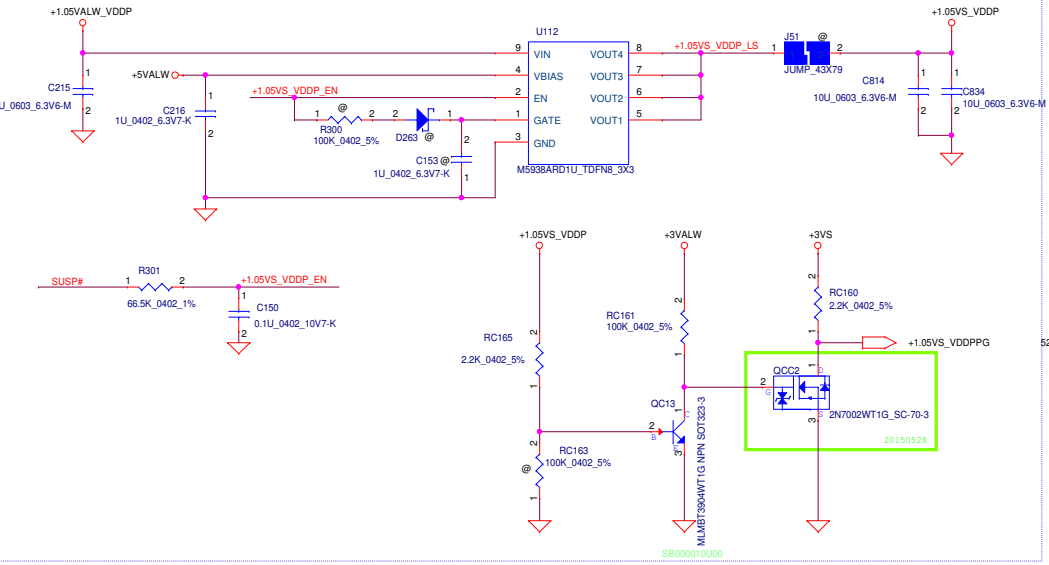
**+1.8VALW to +1.8VS 2A request**

VIN 1.8V (VBIAS=5V), IMAX=6A, Rds=15mohm



**+1.05VALW\_VDDP to +VDDP 10A request**

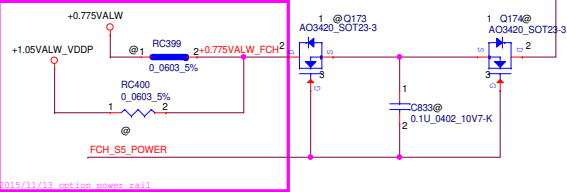
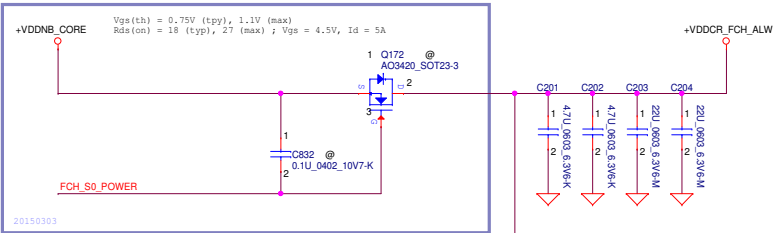
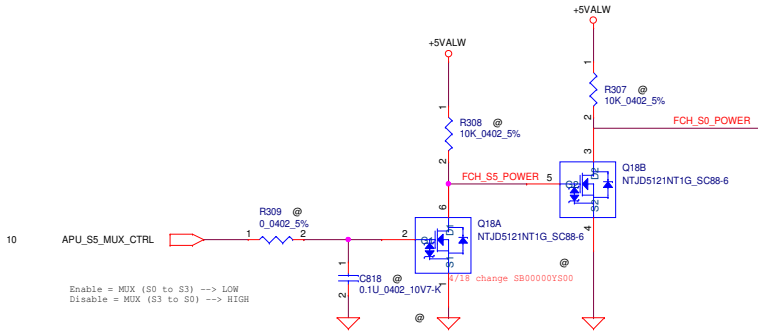
VIN 1.05V (VBIAS=5V), IMAX=10A, Rds=7mohm



Security Classification	LC Future Center Secret Data			Title	
Issued Date	2015/10/5	Deciphered Date	2014/07/01	3VS/5VS/1.1VS/VDDIO_RUN	
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				Date	Monday, August 01, 2016
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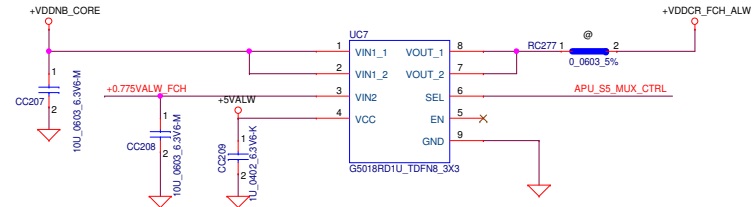
+VDDCR\_FCH\_ALW

During S0: track +VDDNB\_CORE  
During S5/S4/S3: set to +0.775V

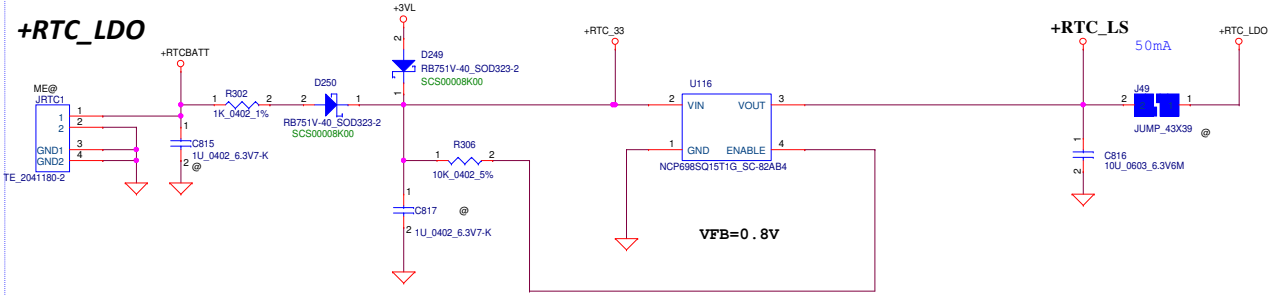


Co-lay

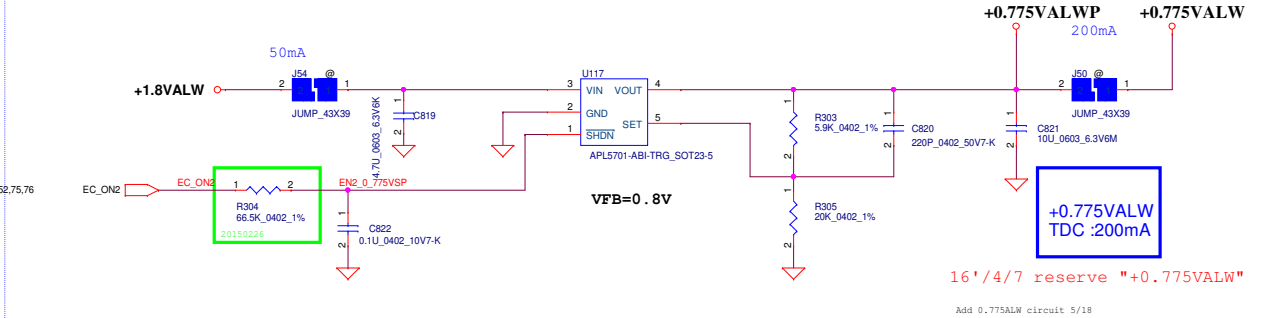
2015/11/05






+RTC\_LDO

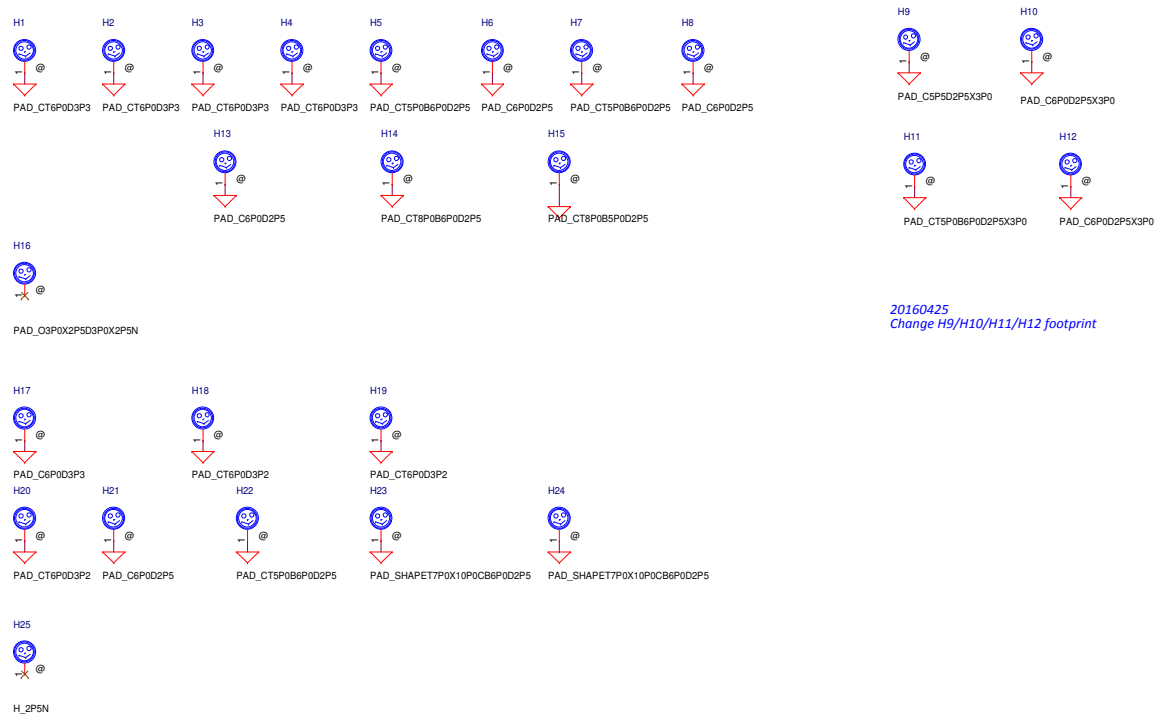


+0.775VALW



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D				D																											
C				C																											
B				B																											
A				A																											
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Date:		Monday, August 01, 2016		Sheet	62 of 80																										
5	4	3	2	1																											

Screw Hole

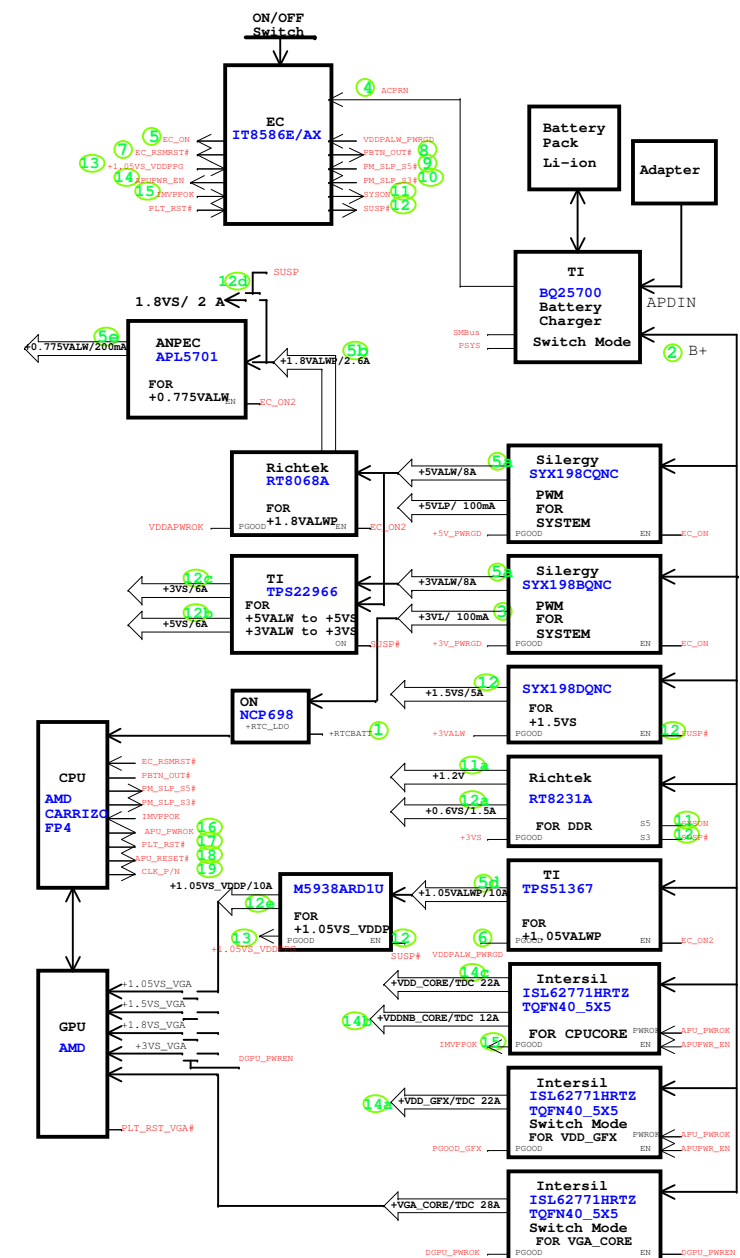
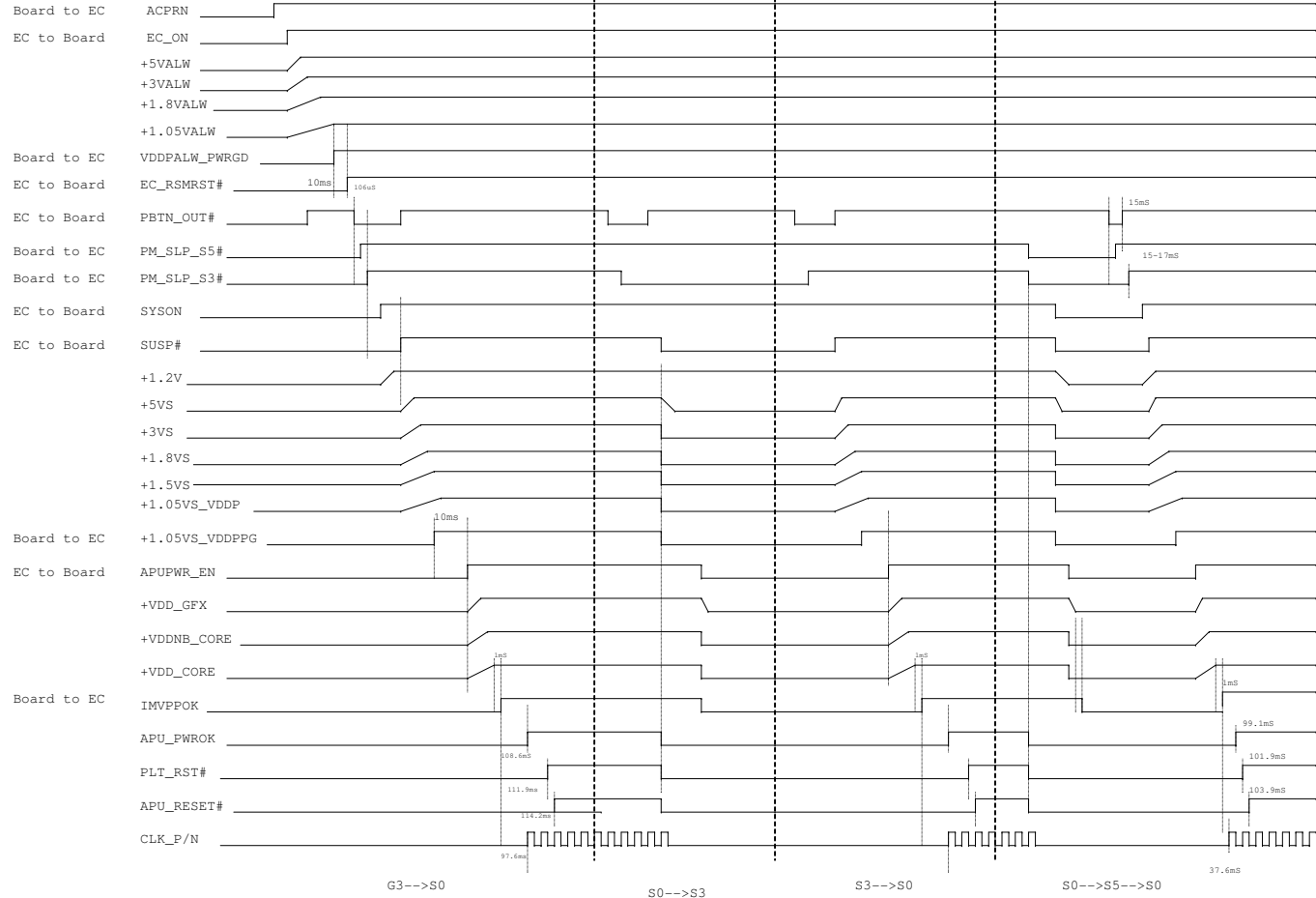



20160425  
Change H9/H10/H11/H12 footprint

Center Zero

PCB Federal Mark PAD





Security Classification	LC Future Center Secret Data		Title	
Issued Date	2015/10/05	Deciphered Date	2014/07/01	

**Power Sequence**

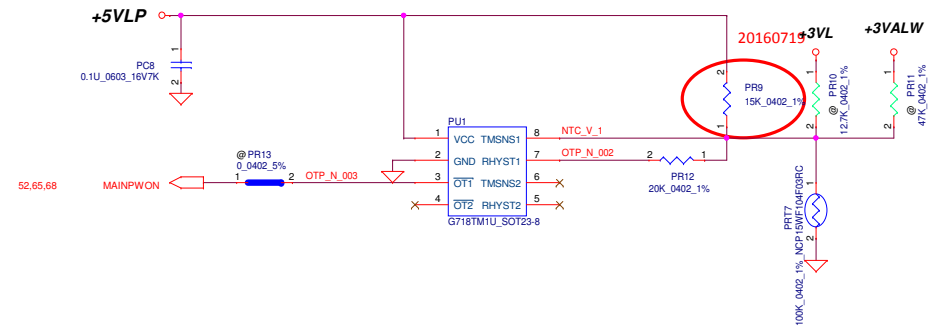
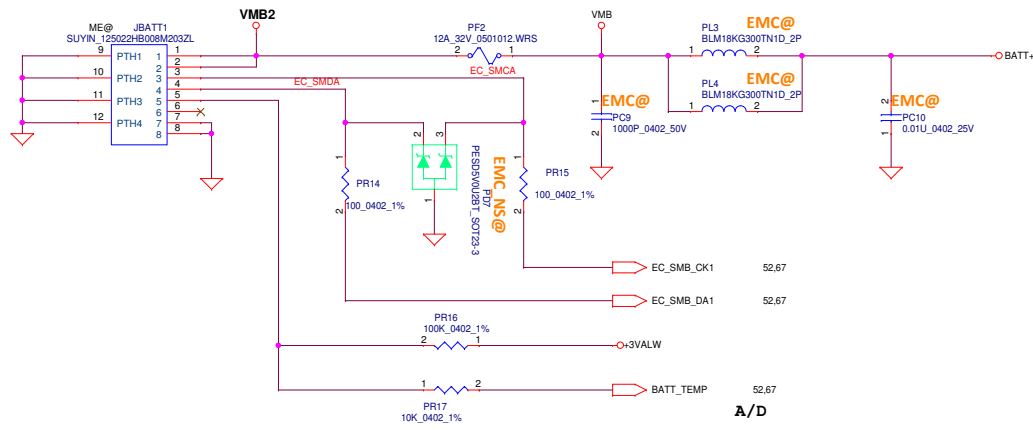
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Size	Document Number	Rev
	<b>NW-A801</b>	1.0





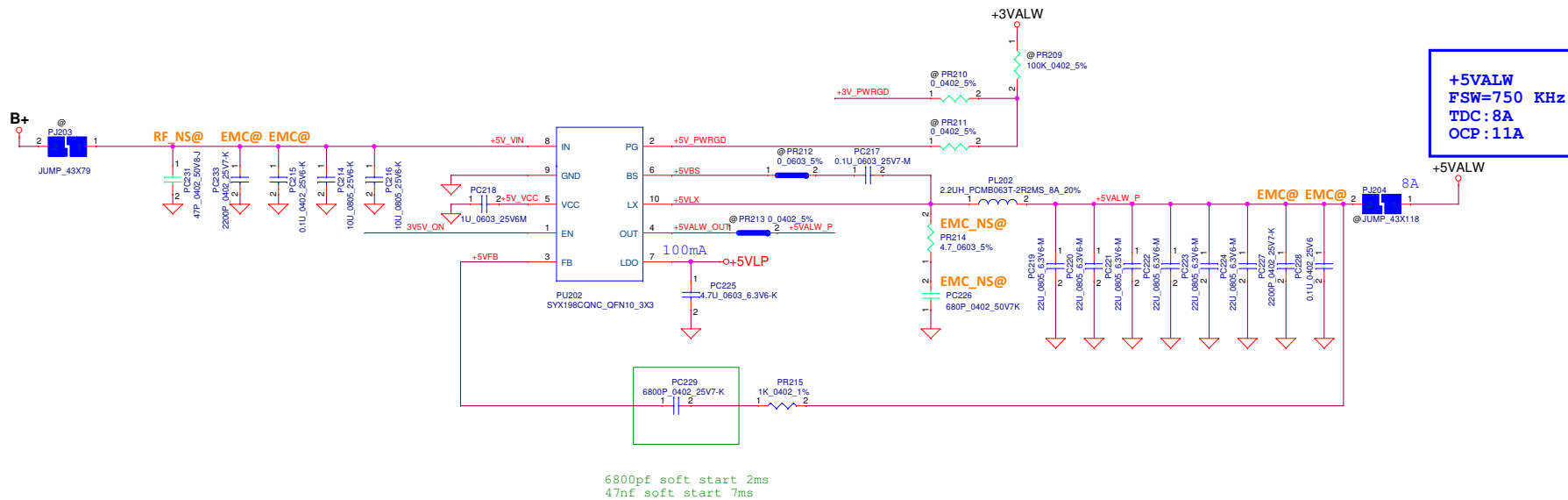
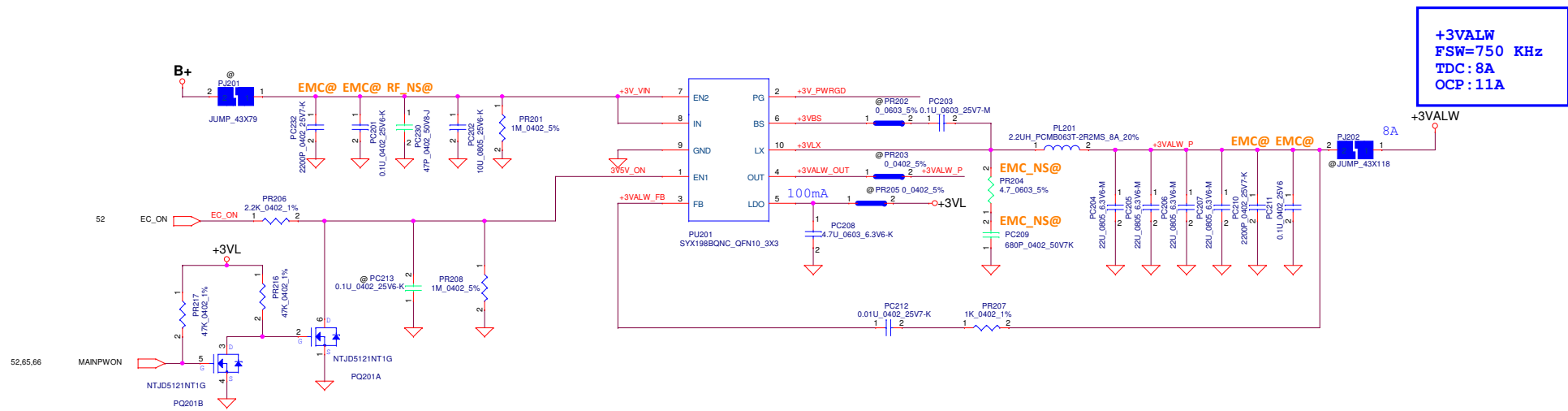
PRT7 under CPU botten side :  
CPU thermal protection at 93 +-3 degree C  
Recovery at 56 +-3 degree C



<Variant Name>

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Issued Date	2013/08/05	Deciphered Date	2014/12/31	Size	Document Number	Rev
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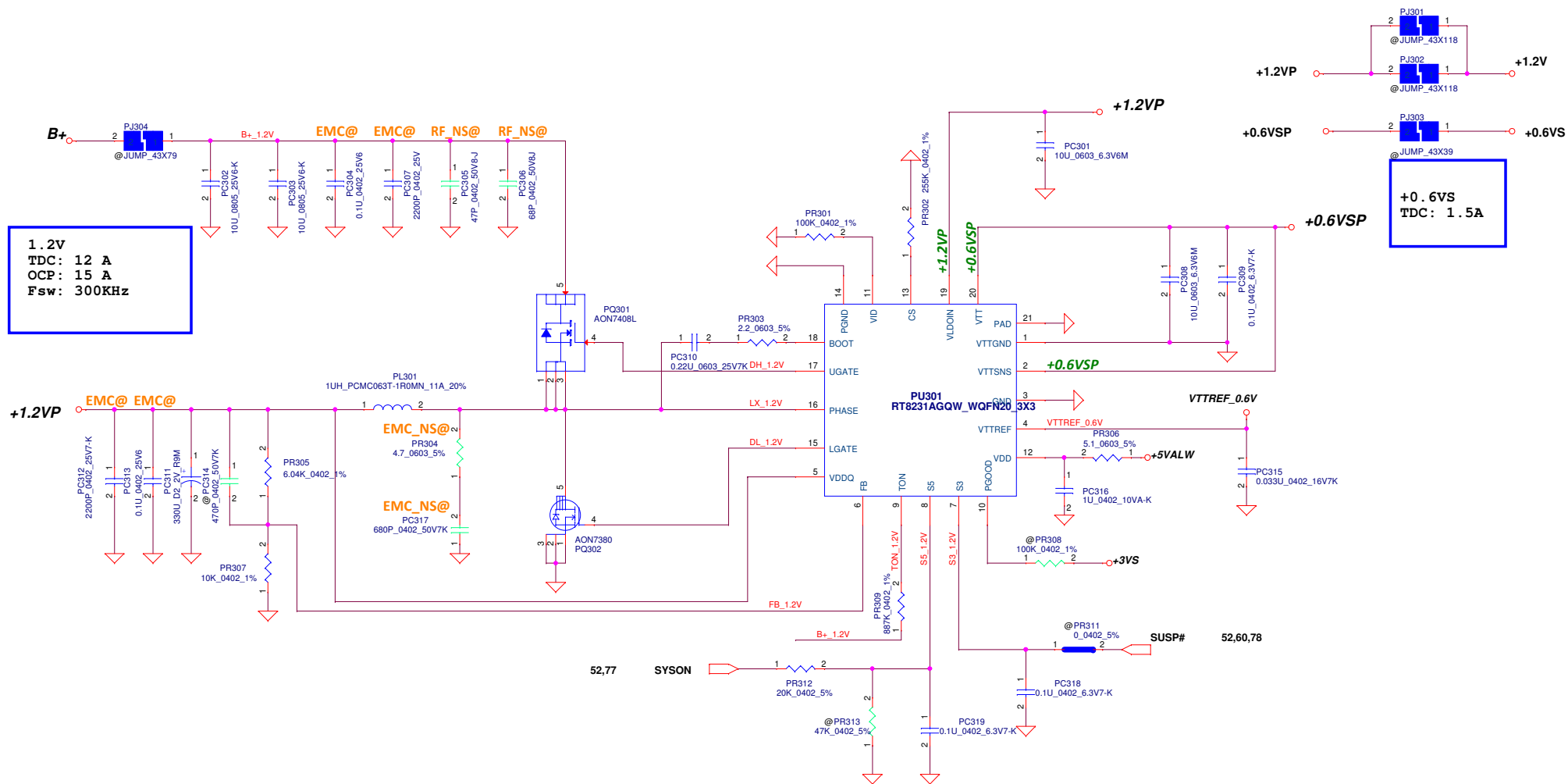




6800pF soft start 2ms  
47nF soft start 7ms

<Variant Name>

Security Classification	LC Future Center Secret Data			Title	3VALWP/5VALWP	Rev 1.0
Issued Date	2013/08/08	Deciphered Date	2013/08/05	Size		
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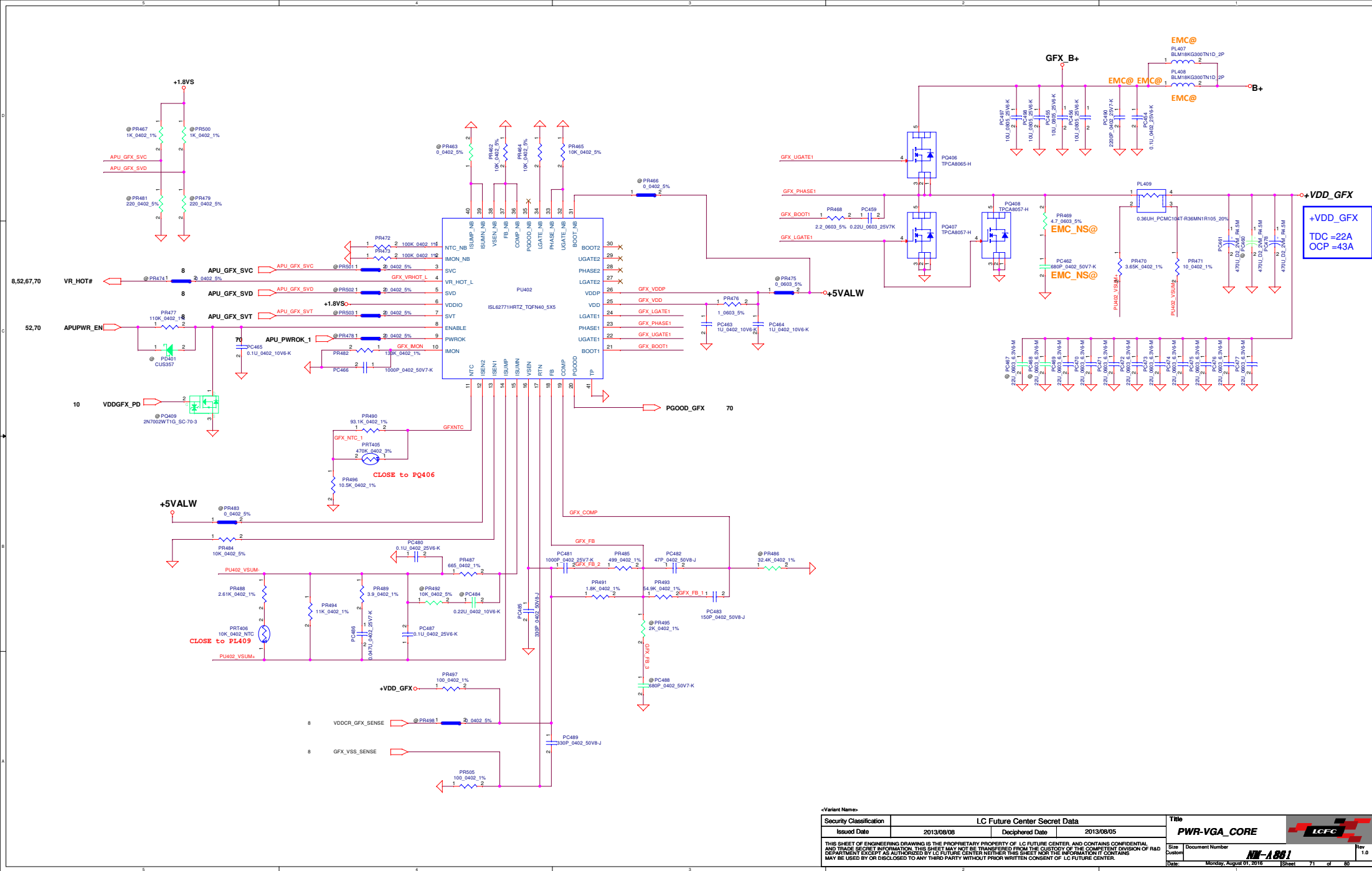
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Security Classification	LC Future Center Secret Data		
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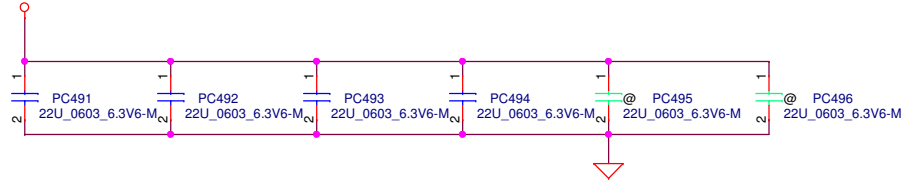
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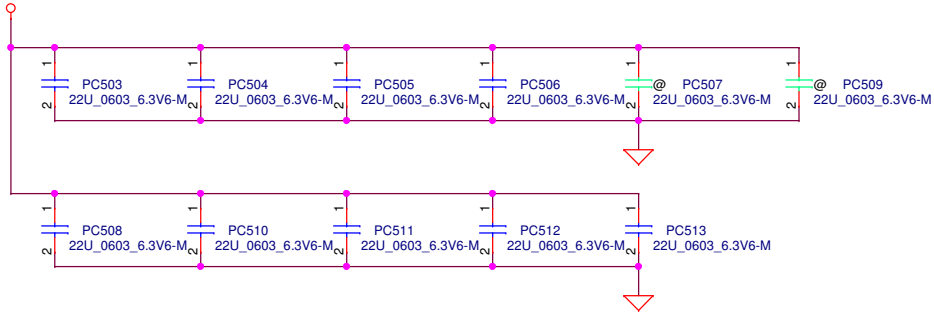





**+VDDNB\_CORE**



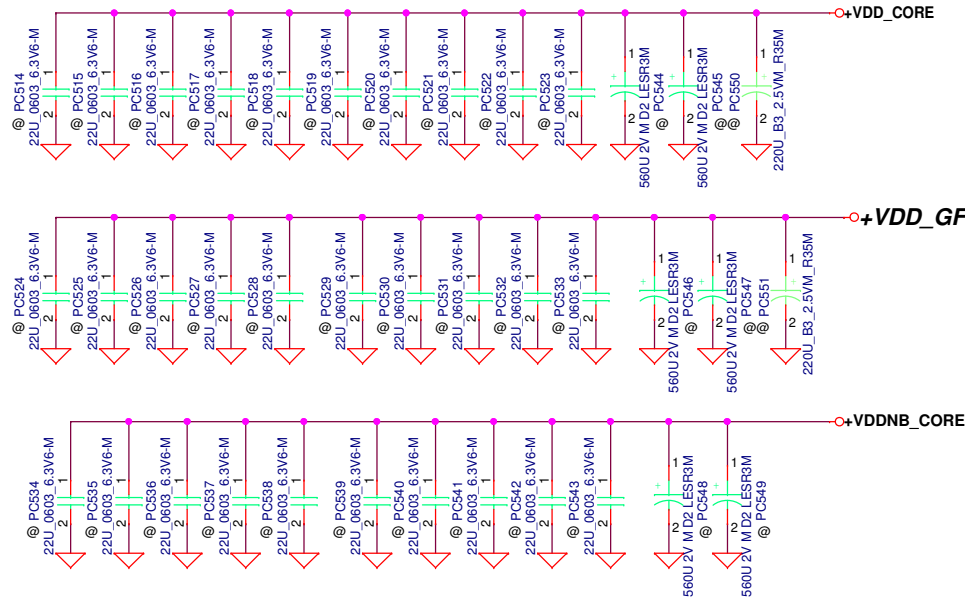
**+VDD\_CORE**



<Variant Name>

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Issued Date	2013/08/01	Deciphered Date	2014/08/01	VCCCPUCORE DECOUPLING			
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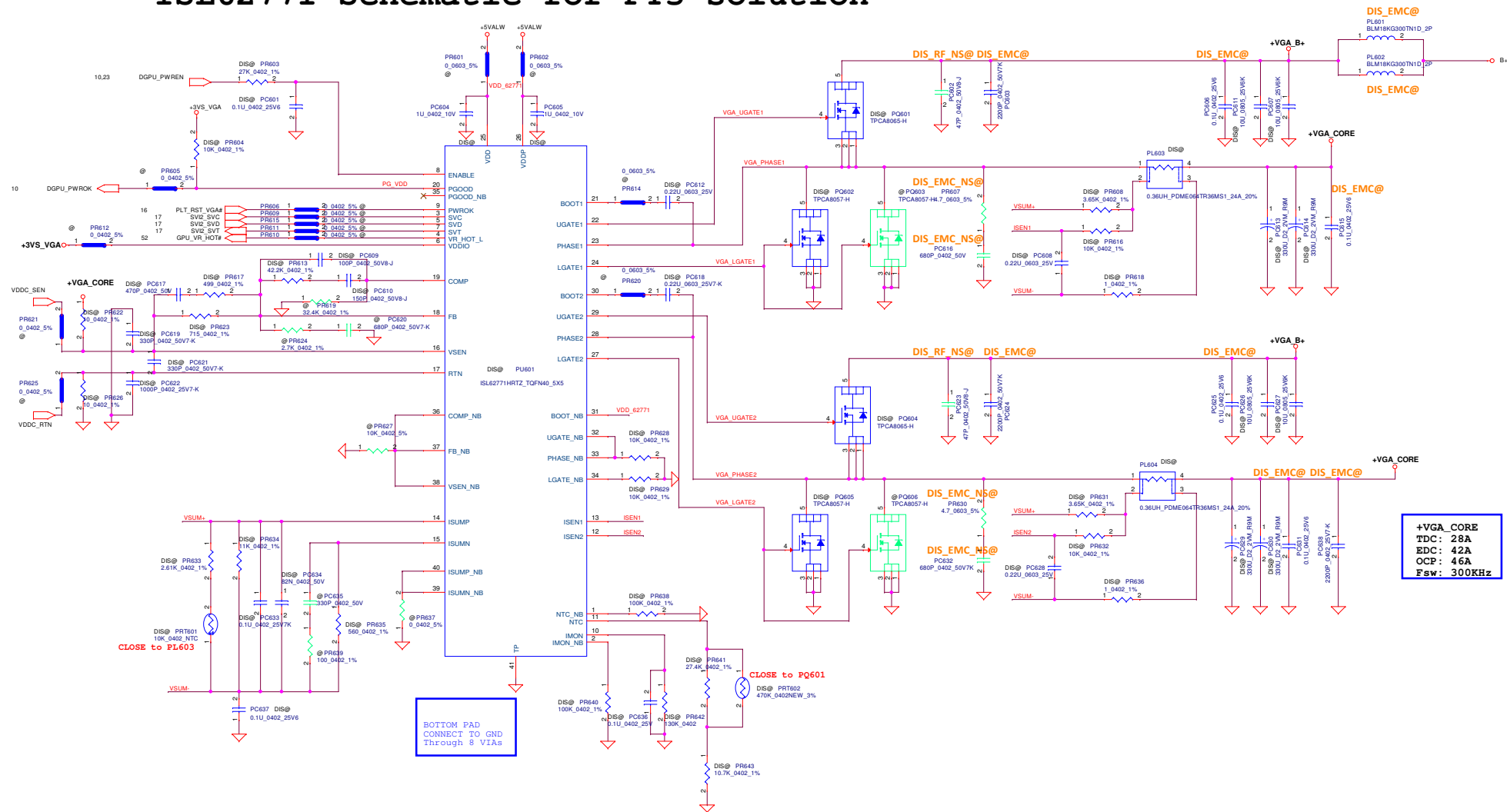



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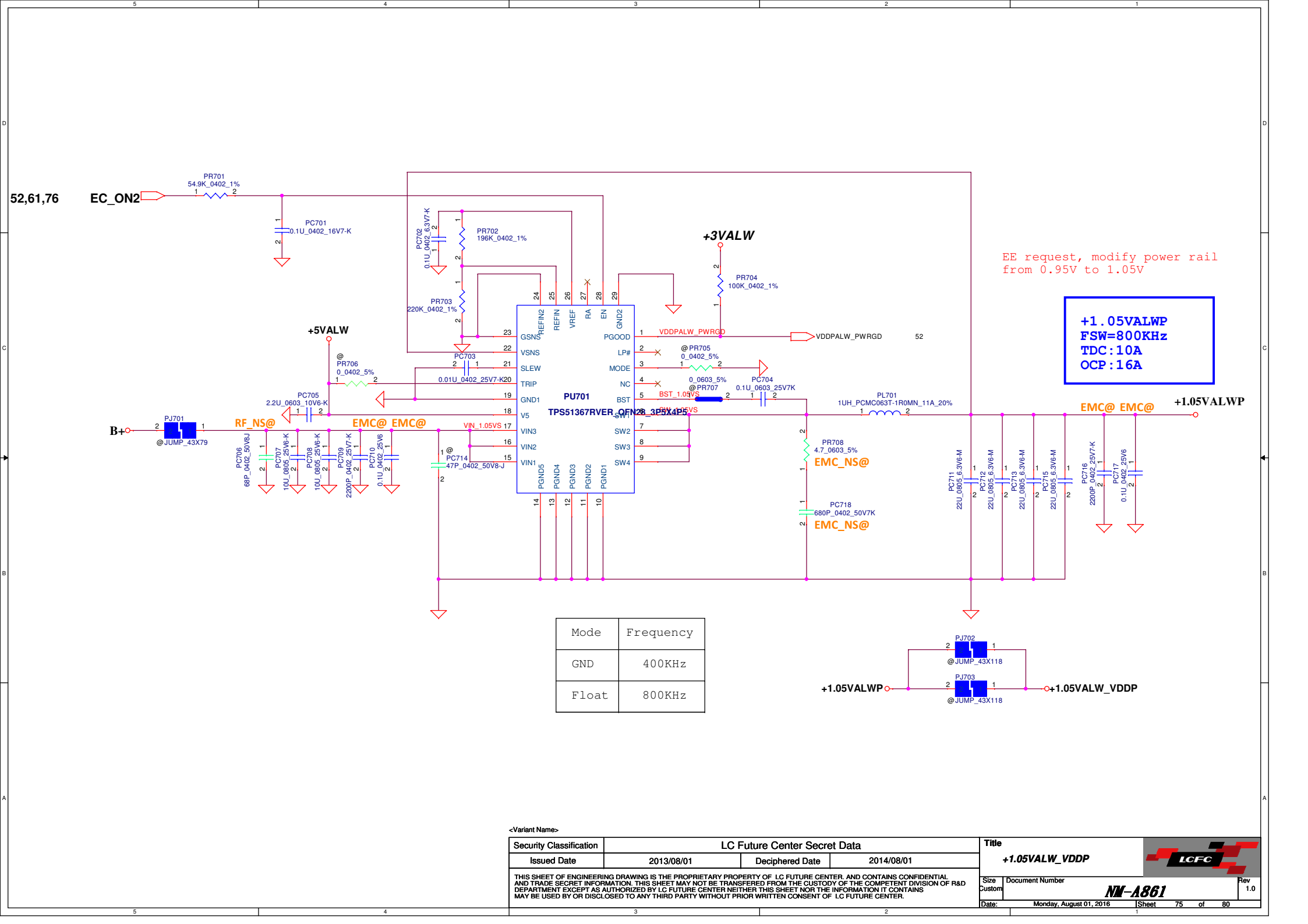
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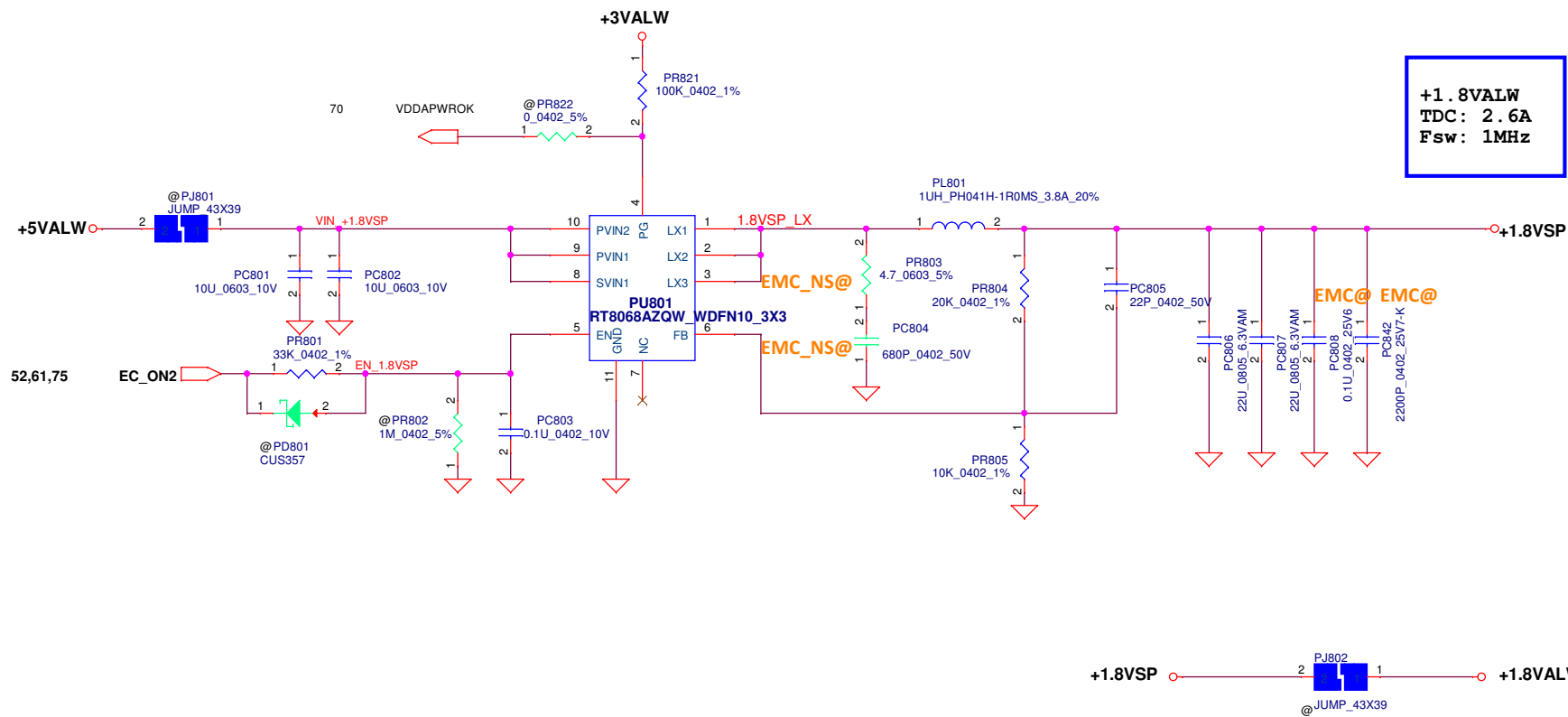
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Size	Document Number	NM-A861		Rev	1.0
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## ISL62771 Schematic for FT3 solution




[Variant Name]								
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Issued Date		2013/08/05	Deciphered Date		2014/12/31		+VGA_CORE	
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				Custom		NEW-A801		1
				Date:		Monday, August 01, 2016 10:09 AM		Page 74 of 80

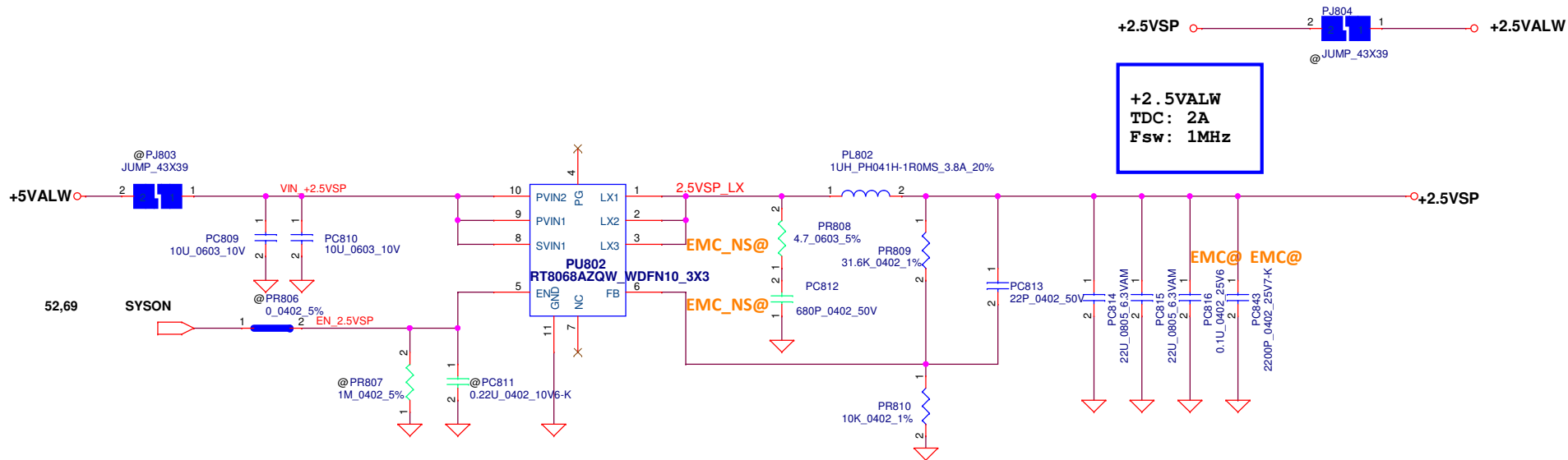





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Title			
+1.8VALW			
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Security Classification	LC Future Center Secret Data			Title		
Issued Date	2013/08/05	Deciphered Date	2014/12/31	+2.5VALW		
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